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[72.	FIRMWARE HUB]
[73.	PORT ANGELES (1 OF 2)]
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[96.	VCCP VREG]
[97.	VCCP VREG]
[98.	VCCP VREG DECOUPLING]
[99.	USB ANTI THEFT
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[103.	VR_THERMAL THROTTLE]
[104.	TEST SITE CAPS]
[105.	BLANK PAGE
[106.	BLANK PAGE

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
1.0	PRELIMINARY		2005				

WOODRIDGE

GRANTSDALE / DDR1 / ICH6 / ATX

FAB A
REV 1.00
TAPE-OUT: WW15.5

POWER SYMBOLS USED:
VCC3
VCC
+12V
-12V

NOTES:

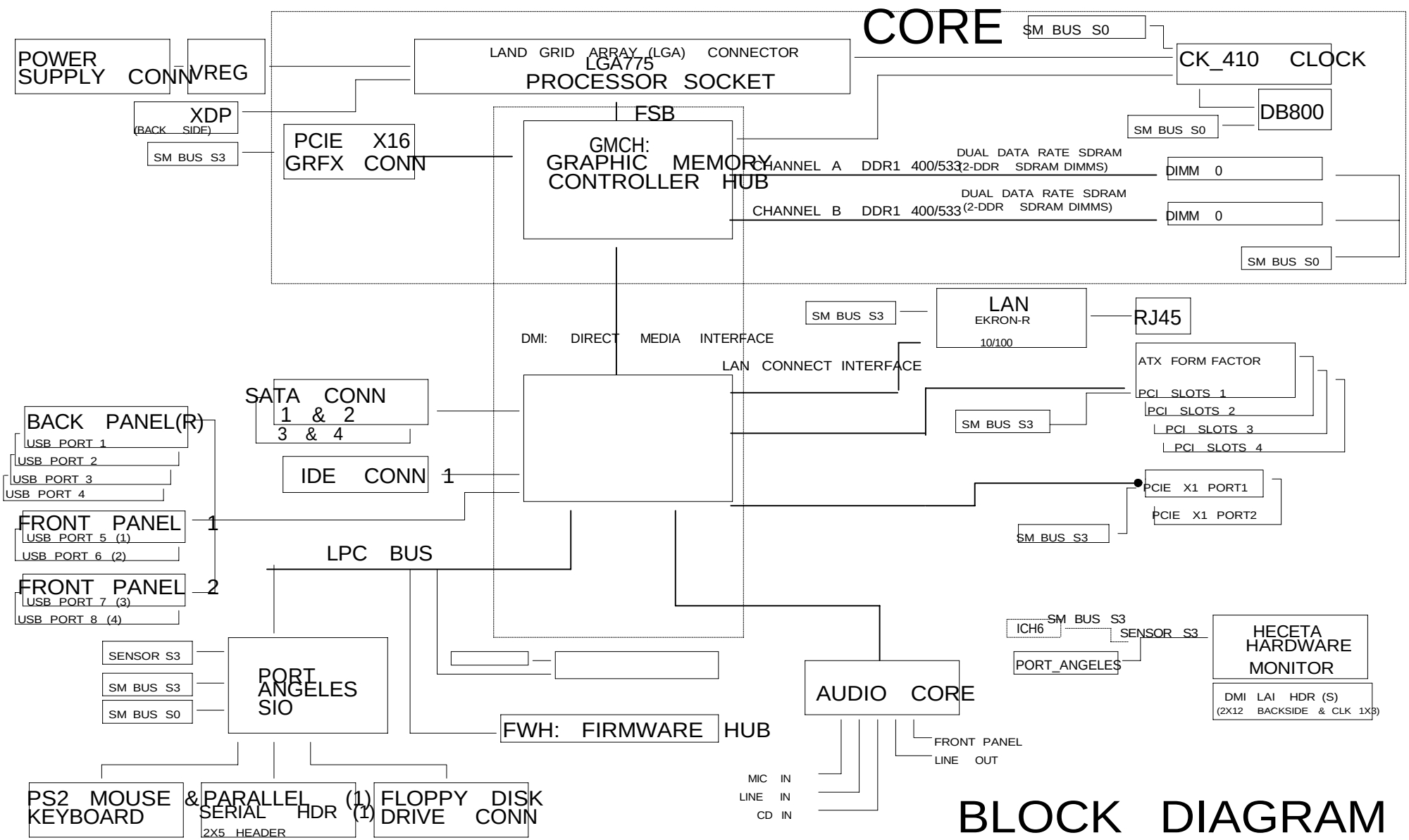
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL § FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

DRAWING
D915PLWDL_FABA.SCH 1.1
Wed Apr 06 22:21:08 2005

BOM RELEASE DATE	03/16/04	PB NUMBER	
SIGNATURE	DATE	int e	3065 BOWERS AVE SANTA CLARA, CA 95051
DRN BY SCLIM		TITLE	SCH, PBA, WOODRIDGE
CHK BY CHTAN	03/16/04		
ENGR APVD			
APVD			
APVD			

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	1/106	1.00

[PAGE_TITLE=INDEX]



BLOCK DIAGRAM

COPIED BLOCK DIAGRAM FROM TGRVP_A, 14/10/2003
BLOCK DIAGRAM UPDATED: 03/26/2005

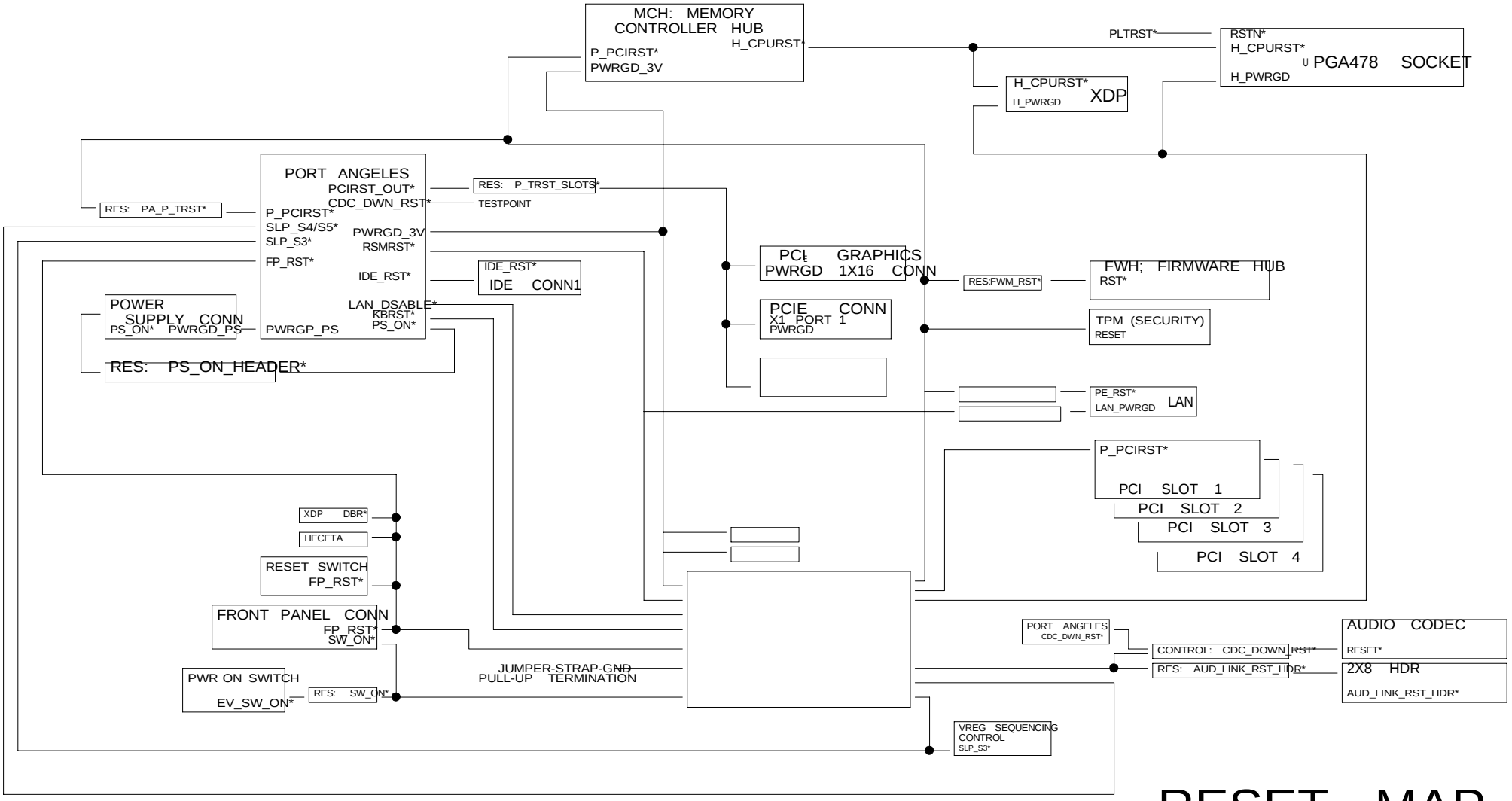
DRAWING
D915PLWDL_FABA.SCH_1.2
Wed Apr 06 22:21:08 2005

[PAGE_TITLE=BLOCK DIAGRAM]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	2	1.00

CORE

AFTER P_PCIRST*, HANDSHAKE (ON HL BUS) BETWEEN ICH/MCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED



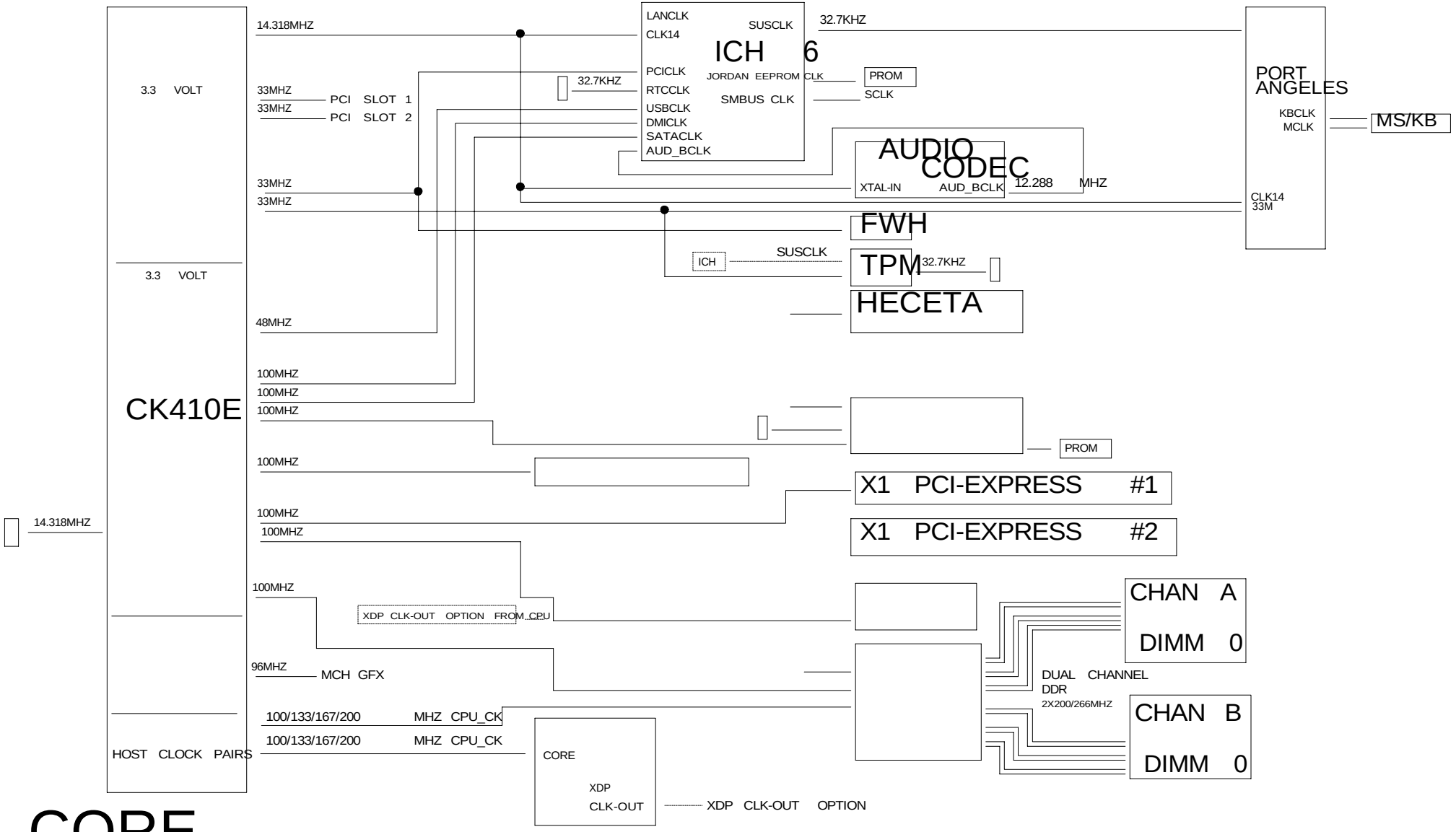
RESET MAP

[PAGE_TITLE=RESET MAP]

COPIED RESET MAP FROM TGRVP_A, 14/10/2003
RESET MAP UPDATED: XX/XX/2003

DRAWING
D915PLWDL_FABA.SCH_1.3
Wed Apr 06 22:21:08 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	3	1.00



CORE

COPIED CLOCK DISTRIBUTION FROM TGRVP_A, 14/10/2003
CLOCK DISTRIBUTION UPDATED: 12/15/2003

CLOCK DISTRIBUTION

DRAWING
D915PLWDL_FABA.SCH_1.4
Wed Apr 06 22:21:09 2005

[PAGE_TITLE=CLOCK DISTRIBUTION]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	4	1.00

ICH 6 FWH

PIN	NAME	WELL	USAGE	DURING RESET	S3/S5	NOTES
GPI[0]		MAIN	P_REQ6*			P/U ON PAGE 54, 2.7K TO VCC
GPI[2]		MAIN	P_REQ5*			P/U ON PAGE 54, 2.7K TO VCC
GPI[2]		MAIN	P_INTE*			P/U ON PAGE 54, 8.2K TO VCC3
GPI[3]		MAIN	P_INTF*			P/U ON PAGE 54, 8.2K TO VCC3
GPI[4]		MAIN	P_INTG*			P/U ON PAGE 54, 8.2K TO VCC3
GPI[5]		MAIN	P_INTH*			P/U ON PAGE 54, 8.2K TO VCC3
GPI[6]		MAIN	1X4_DETECT		OFF	
GPI[7]		MAIN	FP_AUD_DETECT			10K P/D TO 3.3V PG 43
GPI[8]		RESUME	AC_OK (FOR ENERGY LAKE) - NOT USED			10K P/D TO 3.3V STBY PG 43
GPI[9]		RESUME	OC[4]*	HIGH	DRIVEN	
GPI[10]		RESUME	OC[5]*	HIGH	DRIVEN	
GPI[11]		RESUME	SMBALERT*			10K P/U TO 3.3V STBY PG 43
GPI[12]		MAIN	SATA HOT SWAP NOT USED			10K P/D TO GND PG 43
GPI[13]		RESUME	IO_PME*		DRIVEN	
GPI[14]		RESUME	OC[6]*	HIGH	DRIVEN	
GPI[15]		RESUME	OC[7]*	HIGH	DRIVEN	
GPO[16]		MAIN	GNT[6]*	HI-Z	OFF	
GPO[17]		MAIN	GNT[5]*	HI-Z	OFF	
GPO[18]		MAIN	STP_PCI# NOT USE			
GPO[19]		MAIN	OEM_LED0			
GPO[20]		MAIN	STP_PCI#			
GPO[21]		MAIN	NOT ASSIGN			
GPO[22]						
GPO[23]		MAIN	NOT ASSIGN			
GPIO[24]		RESUME	BOARD ID 0	HIGH	OFF	
GPIO[25]		RESUME	INTERNAL VRM STRAP	HIGH	DEFINED	
GPIO[26]		MAIN	SATAGP0			4.7K P/U TO 3.3V PG 39
GPIO[27]		RESUME	BOARD ID 1	HIGH	DEFINED	
GPIO[28]		RESUME	RPS_OFF* NOT USE	HIGH	DEFINED	10K P/D TO GND PG 43
GPIO[29]		MAIN	SATAGP1			4.7K P/U TO 3.3V PG 39
GPIO[30]		MAIN	SATAGP2			4.7K P/U TO 3.3V PG 39
GPIO[31]		MAIN	SATAGP3			4.7K P/U TO 3.3V PG 39
GPIO[32]		MAIN	NOT USED	HIGH	OFF	
GPIO[33]		MAIN	BOARD ID 2	HIGH	OFF	
GPIO[34]		MAIN	BOARD ID 3			
GPI[40]		MAIN	REQ[4]*			
GPI[41]		MAIN	LDRQ[1]*			
GPO[48]		MAIN	GNT[4]*			
GPO[49]		CPU	CPUPWRGD			
GPI4		CORE	NORM	INPUT		
GPI3		CORE	MFG_MODE*	INPUT		
GPI2		CORE	BSKU4	INPUT		
GPI1		CORE	BAT_WARN	INPUT		
GPI0		CORE	DMA66_DETECT_PRI	INPUT		HI/LOW BIOS CONFIG FOR IDE PRI (FEATURE IS DEFAULT LOW)

PORT ANGELES

		PA1.5	PA3.0			
GPO0		NA	SENSOR_SDA	OUTPUT		
GPO1		NA	FANTACH3	INPUT		
GPO2		GPO_LAN_DISABLE	FANTACH4	INPUT		
GPO3		NA	FANPWM1	OUTPUT		
GPO4		BSKU5/1_WATT	FANPWM2	OUTPUT		
GPO5		NA	FANPWM3	OUTPUT		
GPI6		FAN_TACH1	FAN_TACH1	INPUT		
GPI7		FAN_TACH2	FAN_TACH2	INPUT		
GPIO10		5V_DDCSDA	5V_DDCSDA	INPUT		
GPIO11		5V_DDCSCL	5V_DDCSCL	INPUT		
GPIO12		3V_DDCSDA	3V_DDCSDA	INPUT		
GPI013		3V_DDCSCL	3V_DDCSCL	INPUT		
GPI14		CDC_DWN_ENAB*	CDC_DWN_ENAB*	INPUT		2X12_DETECT
IO_PME*		IO_PME*		OUTPUT		
GRN_LED		GRN_LED		OUTPUT		
YLW_LED		YLW_LED		OUTPUT		

MULTI-PLEXED GPIO PINS ON PORT ANGELES USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON PORT ANGELES ARE NOT IDENTIFIED HERE
TOTAL OF (37) POSSIBLE GPIO PINS ON PORT ANGELES.

IRQ ROUTING TABLE

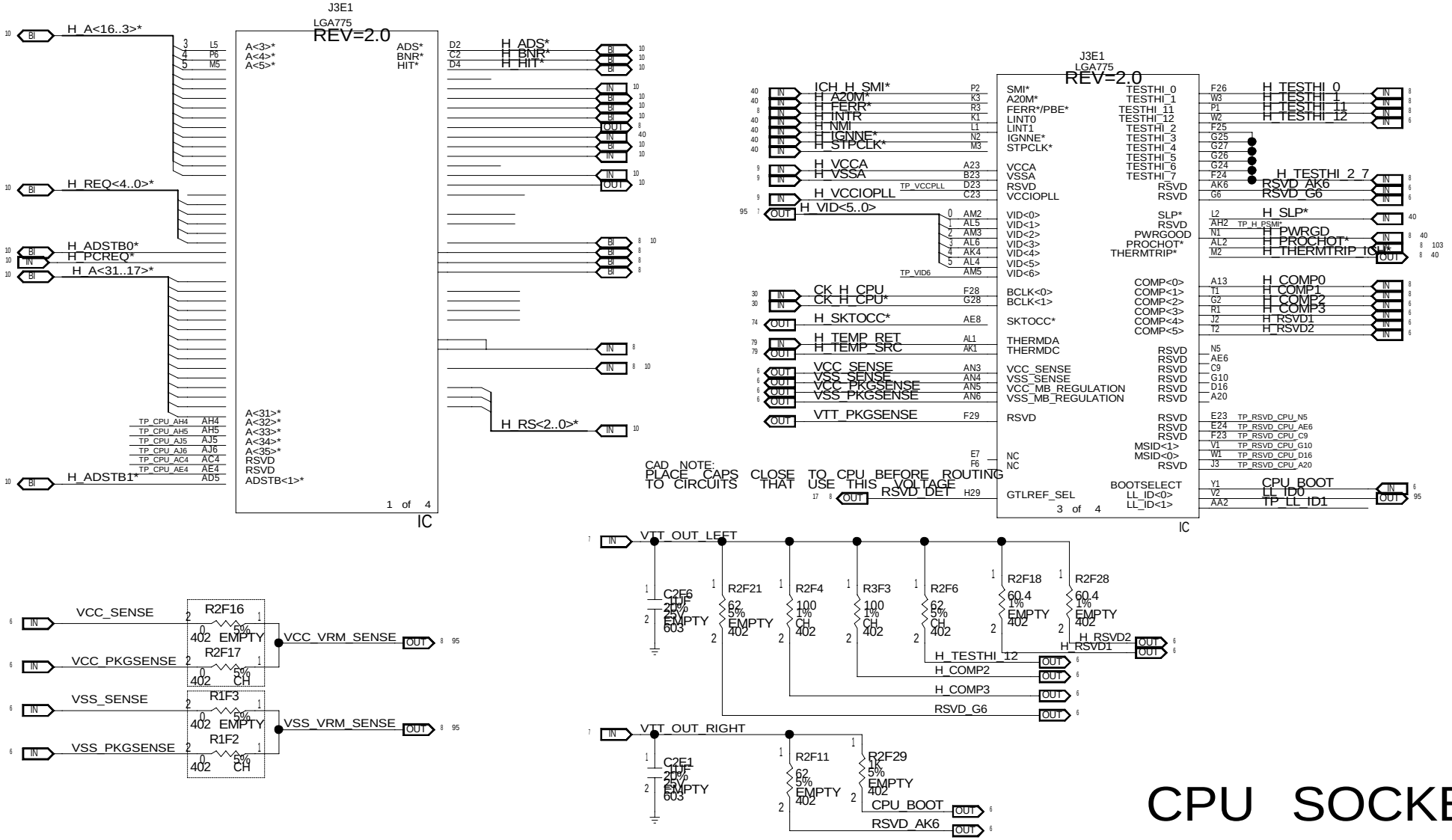
CONFIRMED ++++++++++++++++++++++++++++++++++++ PCI-EXPRESS @@@@@@@@@@@@@@ NOT CONFIRMED @@@@@@@@@@@@@@

		SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	X1_2	X16	X1_1	LAN	USB1-F0	USB1-F1	USB1-F2	USB1-F3	USB #2	SMBUS	AZALIA
P_INTA*				IRQD				IRQA						IRQD			
P_INTB*				IRQC					IRQA								IRQA
P_INTC*				IRQA	IRQB								IRQC				
P_INTD*				IRQB	IRQA							IRQB				IRQB	
P_INTE*		IRQD	IRQC							IRQA							
P_INTF*		IRQA	IRQB		IRQC												
P_INTG*		IRQB	IRQA		IRQD												
P_INTH*		IRQC	IRQD								IRQA				IRQA		
REQ/GNT		1	2	3	4												
IDSEL		16	17	18	19					24							

COPIED INFO FROM TGRVP_A, 10/14/2003
INFORMATION UPDATED: 12/12/2003

GPIO, IRQ, IDSEL MAPS

DRAWING
D915PLWDL_FABA.SCH_1.5
Wed Apr 06 22:21:09 2005 [PAGE_TITLE=GPIO, IRQ, IDSEL MAP]



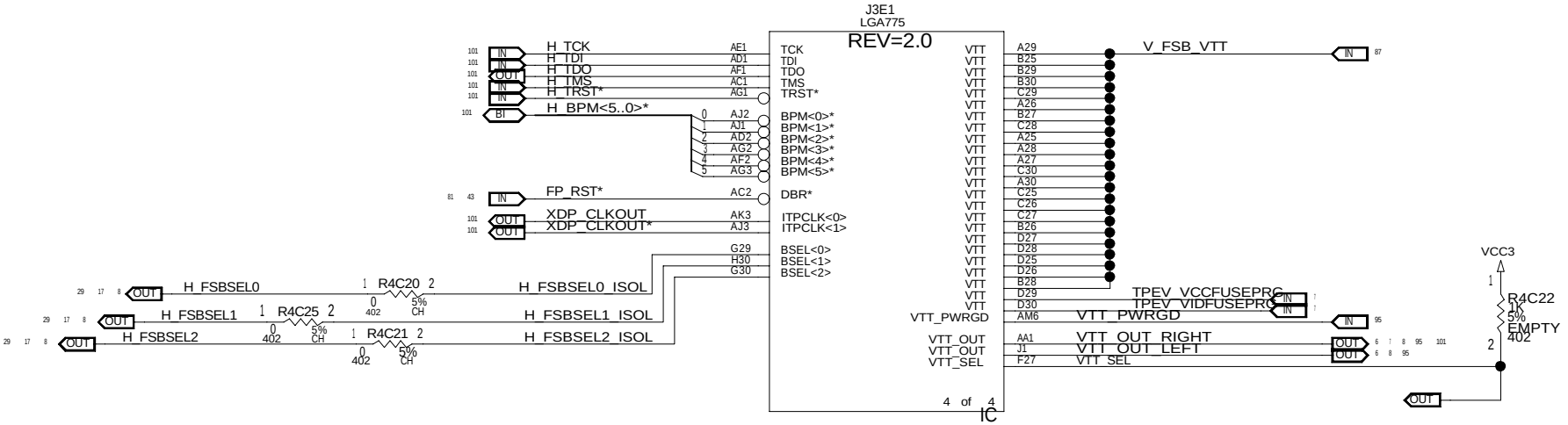
CPU SOCKET

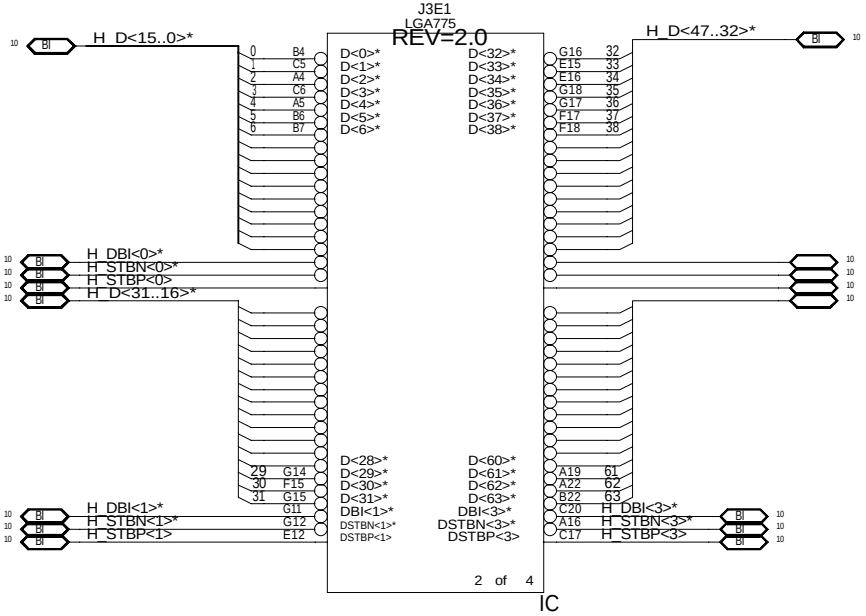
[PAGE_TITLE=CPU-SOCKET]

CORE PAGE

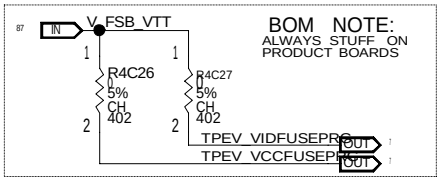
DRAWING
D915PLWDL_FABA.SCH_1.6
Thu Apr 07 00:58:48 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	6	1.00

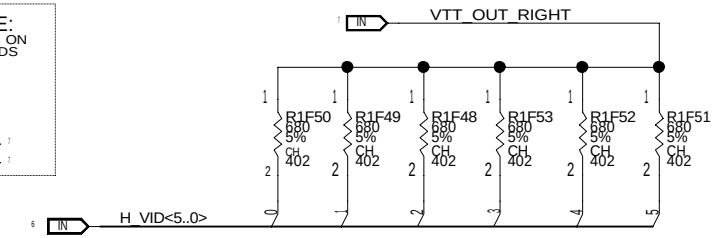




VCCP=AG22,K29,AM26,AL8,AE12,AE11
VCCP=W23,W24,W25,T25,Y28,AL18,AC25,W30,Y30,AN14,AD28,Y26,AC29,M29,U24,J23,AC27,AM18,AM19,AB8
VCCP=AC26,J8,J28,T30,AM9,AF15,AC8,AE14,N23,W29,U29,AC24,AC23,Y23,AN26,AN25,AN11,AN18,Y27,Y25
VCCP=AD24,AE23,AE22,AN19,V8,K8,AE21,AM30,AE19,AC30,AE15,M30,K27,M24,AN21,T8,AC28,N25,AE18,W26
VCCP=AD25,M8,N30,AD26,AJ26,AM29,M25,M26,L8,U25,Y8,AJ12,AD27,U23,M23,AG29,N27,AM22,U28,K28
VCCP=U8,AK18,AD8,K24,AH28,AH21,AK12,AH22,T29,AM14,AM25,AE9,Y29,AK25,AK19,AG15,J22,T24,AG21,AM21
VCCP=J25,U30,AL21,AG25,AJ18,J19,AH30,J15,AG12,AJ22,J20,AH18,AH26,W27,AL25,AN8,AH14,U27,T23,R8
VCCP=AK22,AN29,AG11,AK26,J10,AJ15,AG26,AN9,AH15,AF18,AL15,J26,J18,J21,AG27,AK15,AF11,AD23,AM15,AF8
VCCP=AK21,AG30,AJ21,AM11,AL11,AJ11,K30,AL14,AN30,AH25,AL12,AJ9,AK11,AG14,N29,AL30,AJ25,AH9,J29,J11
VCCP=K25,P8,K23,AL19,AM8,T26,N28,AH12,AL22,AN15,AJ8,U26,AJ19,T27,AK8,AN12,AG9,N26,AF9,AF22
VCCP=AH11,AJ14,AH19,AH29,AH27,AG28,AL26,AM12,J24,J13,T28,W28,J12,J27,AG19,AL9,AD30,AF21,Y24,AK14
VCCP=J9,M27,AF14,J30,AG18,AA8,AG8,AL29,AD29,W8,AH8,N24,AN22,J14,K26,AF19,N8,AF12,M28,AK9
GND=C10,D12,AM7,C24,K2,C22,AN1,B14,K7,AE16,B11,AL10,AK23,H12,AF7,AK7
GND=H7,E14,L28,Y5,E11,AL16,AL24,AK13,AL3,D21,AL20,D18,AN2,AK16,AK20,AM27,AM1,AL13,AL17,C19
GND=E28,AH7,AK30,D24,AL23,A12,L25,J7,AE28,AE29,K5,J4,AE30,AN20,AE10,AE24,AM24,AN23,H9,H8
GND=H13,AC6,AC7,AH6,C16,AM16,AE25,AE27,AJ28,AJ7,F19,AH13,AD7,AH16,AK17,E17,AH17,AH20,AE5,AH23
GND=AE7,AM13,AH24,AJ30,AJ10,AF3,AK5,AJ16,AF6,AK29,AJ17,F22,AH3,AK10,AM10,F16,AJ23,F13,AG7,F10
GND=L26,AD4,H11,L24,L23,AM23,A15,AH10,B24,L3,H27,A21,AE2,AJ29,A24,AK27,AK28,B20,AM20
GND=H26,B17,H25,H24,AA3,AA7,H23,AA6,H10,H22,H21,H20,H19,H18,AB7,H17,AJ24,AM17,AC3,H14
GND=P28,V6,AK2,P27,P26,AM28,AJ13,W4,P25,AJ20,W7,P23,C7,Y2,L30,L29,D15,AL27,Y7,L27
GND=AA29,N6,N7,AA28,AN13,AA27,AA26,P4,AA25,AA24,P7,E26,V30,R2,V29,V28,R5,V27,R7,E20
GND=AN10,V25,T3,V24,V23,T6,AL7,E25,U1,R29,R28,R27,R26,R25,U7,R24,R23,P30,V3,P29
GND=AF16,AE10,AF13,H6,A18,A2,E2,D9,C4,A6,D6,D5,A9,D3,B1,B5,B8,AJ4,AE26,AH1
GND=E29,V7,C13,AK24,AB30,L6,L7,AB29,M1,AB28,AN17,AB27,AB26,AN16,M7,AB25,AB24,AB23,N3,AA30
GND=F4,AG10,AE13,AF30,H28,F7,AF29,AF28,G1,AF27,AF26,AF25,AN28,AN27,AF24,AF23,AG24,AF17,AN24,H3
GND=AN7,P24,AE20,AE17,E27,T7,R30,AJ27,AB1,AM4,V26,AA23,AL28,AF20,AG23,AG20,E8,AG17,AG16,AG13
NC=F6,Y3,AE3,E7,B13,D14,E6,D1,E5,



BOM NOTE:
ALWAYS STUFF ON
PRODUCT BOARDS



DRAWING
D915PLWDL_FABA.SCH_1.7
Thu Apr 07 00:59:35 2005

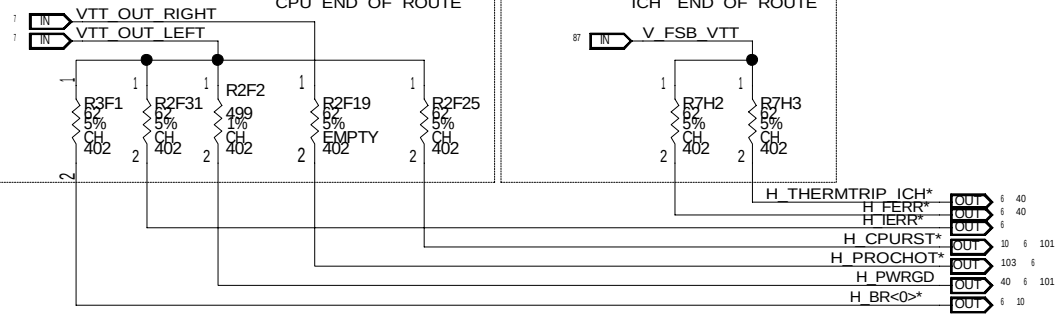
[PAGE_TITLE=CPU-SOCKET]

CORE PAGE

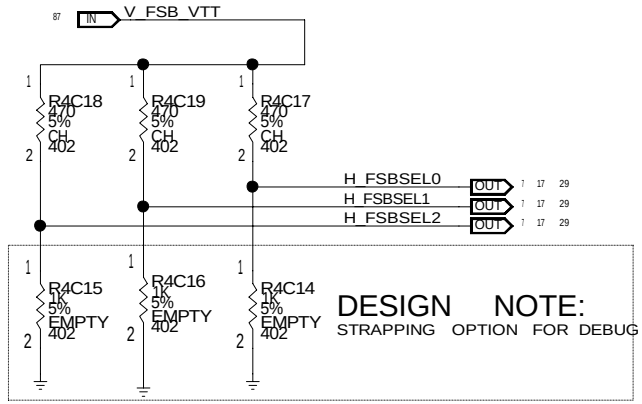
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	7	1.00

CAD NOTE: PLACE AT CPU END OF ROUTE

CAD NOTE: PLACE AT ICH END OF ROUTE

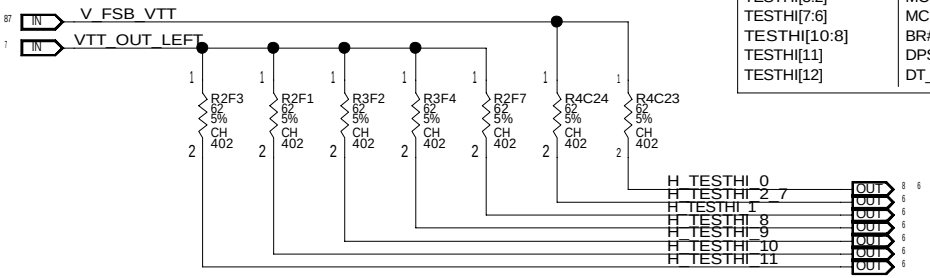


CPU SIGNAL TERMINATION

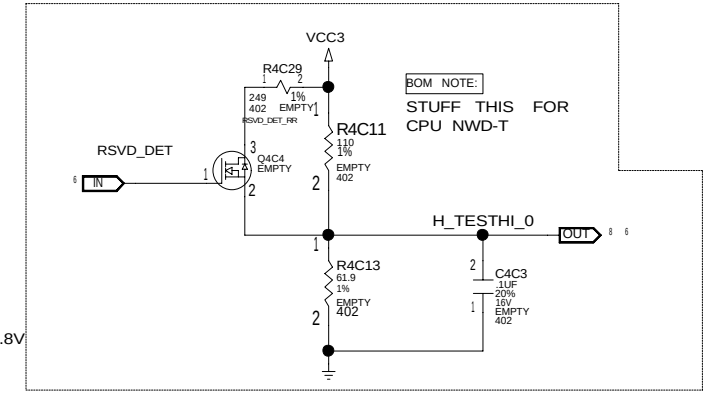


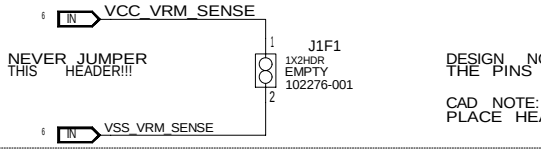
DESIGN NOTE:
STRAPPING OPTION FOR DEBUG

TESTHI PULLUPS



TESTHI PIN NAME MAPPING	
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	DPSLP#
TESTHI[12]	DT_SVR#





NEVER JUMPER THIS HEADER!!!

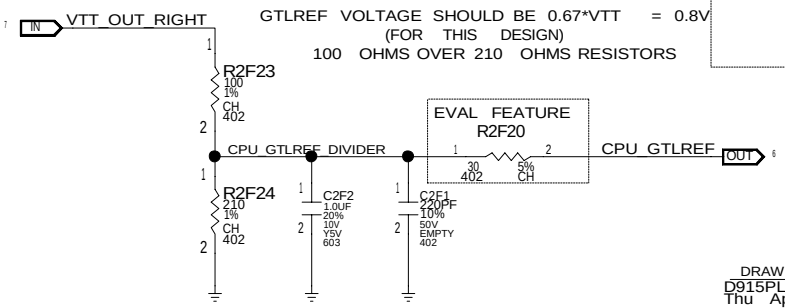
DESIGN NOTE:
THE PINS WILL BE USED AS TEST/PROBE POINTS ONLY.

CAD NOTE:
PLACE HEADERS AS CLOSE TO CPU PINS AS POSSIBLE

PRECISION FSB COMPENSATION RESISTORS

PLACE RESISTORS OUTSIDE SOCKET CAVITY
IF NO ROOM FOR VARIABLE RESISTOR DON'T PLACE.

GTLREF VOLTAGE SHOULD BE 0.67*VTT = 0.8V
(FOR THIS DESIGN)
100 OHMS OVER 210 OHMS RESISTORS



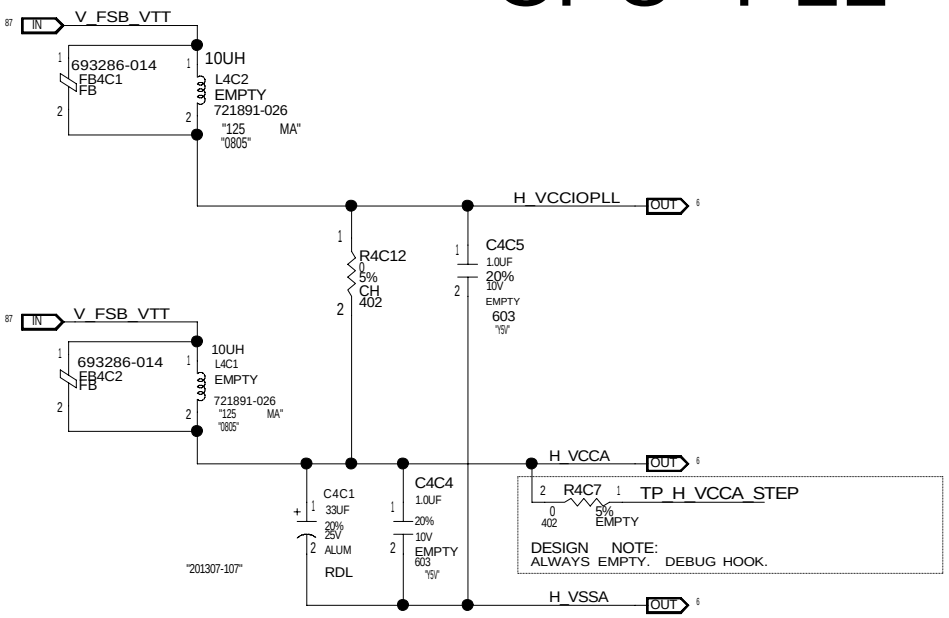
CORE PAGE

[PAGE_TITLE=CPU TERMINATION & MISC]

DRAWING
D915PLWDL_FABA.SCH_1.8
Thu Apr 07 00:58:58 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	8	1.00

CPU PLL SUPPLY FILTER



CAD NOTE:
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

[PAGE_TITLE=CPU ANALOG PLL FILTER]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.9
Thu Apr 07 00:59:07 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	9	1.00

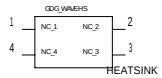
J4F1 NC EMPTY

J6D1 NC EMPTY

J4D1 NC EMPTY

J6F1 NC EMPTY

HS6D1

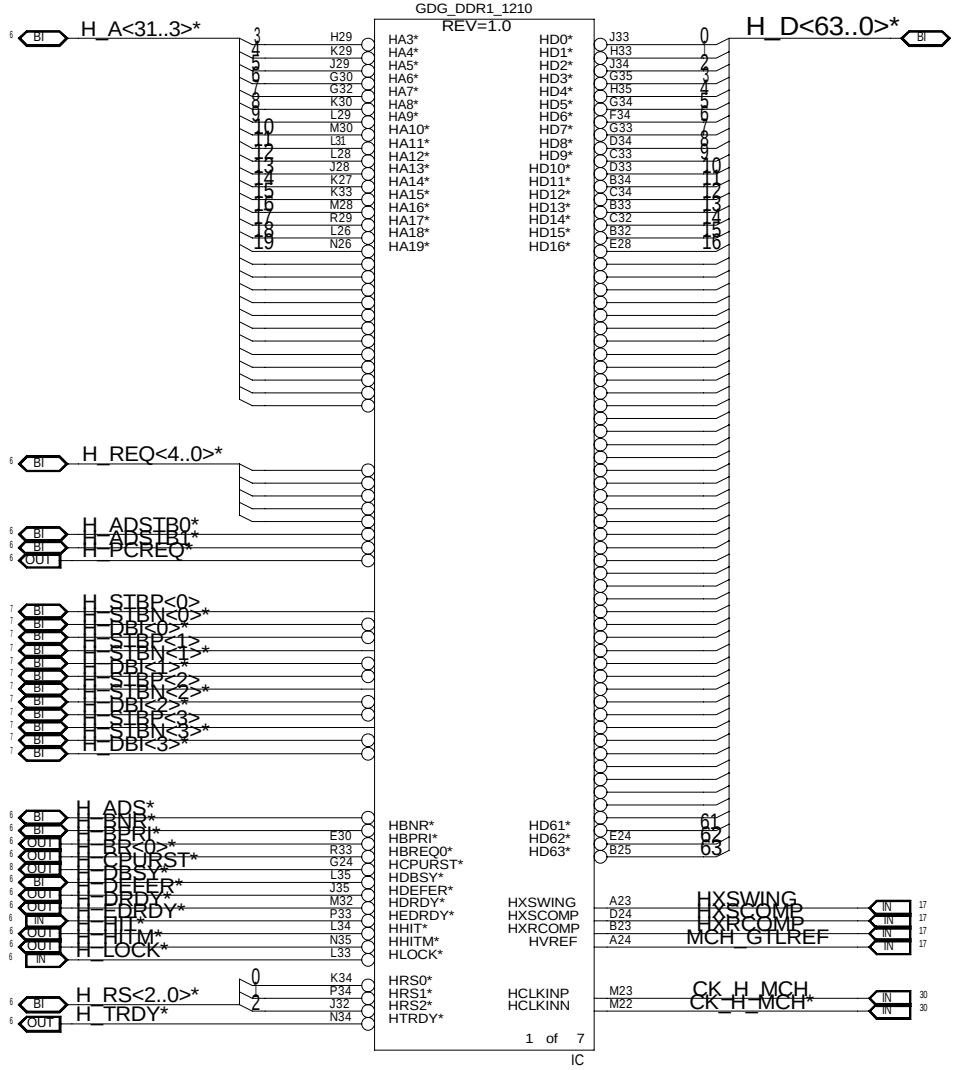


C45196-001

WAVE SOLDER HEAT-SINK = WSHS

NOTE :
USE D10665-001 FOR GMCH

U6D1
GDG_DDR1_1210
REV=1.0



[PAGE_TITLE=MCH SECTIONS PAGE 1 OF 6]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.10
Thu Apr 07 00:59:12 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	10	1.00

FIN=NB

BOM=CORE

CR-11 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE11

SIGNAL NAMING CONVENTION

EXP: PCI EXPRESS

DMI: DIRECT MEDIA INTERFACE

ITP: ICH TRANSMIT POSITIVE

ITN: ICH TRANSMIT NEGATIVE

IRP: ICH RECEIVE POSITIVE

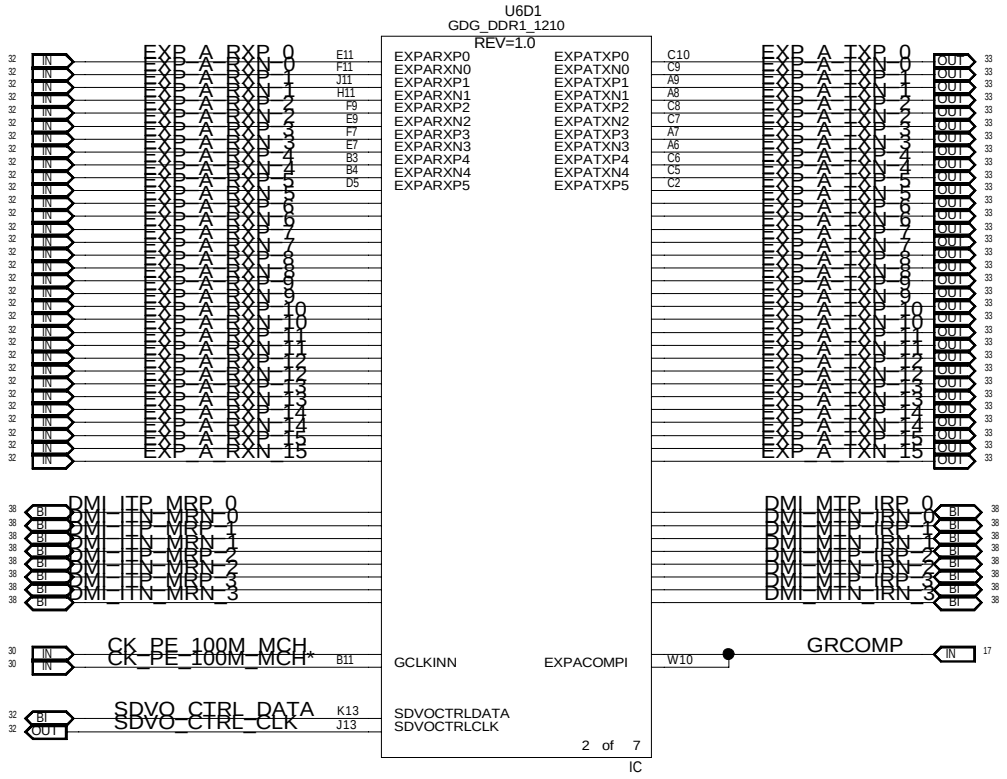
IRN: ICH RECEIVE NEGATIVE

MTP: MCH TRANSMIT POSITIVE

MTN: MCH TRANSMIT NEGATIVE

MRP: MCH RECEIVE POSITIVE

MRN: MCH RECEIVE NEGATIVE



SDVO CTRL DATA

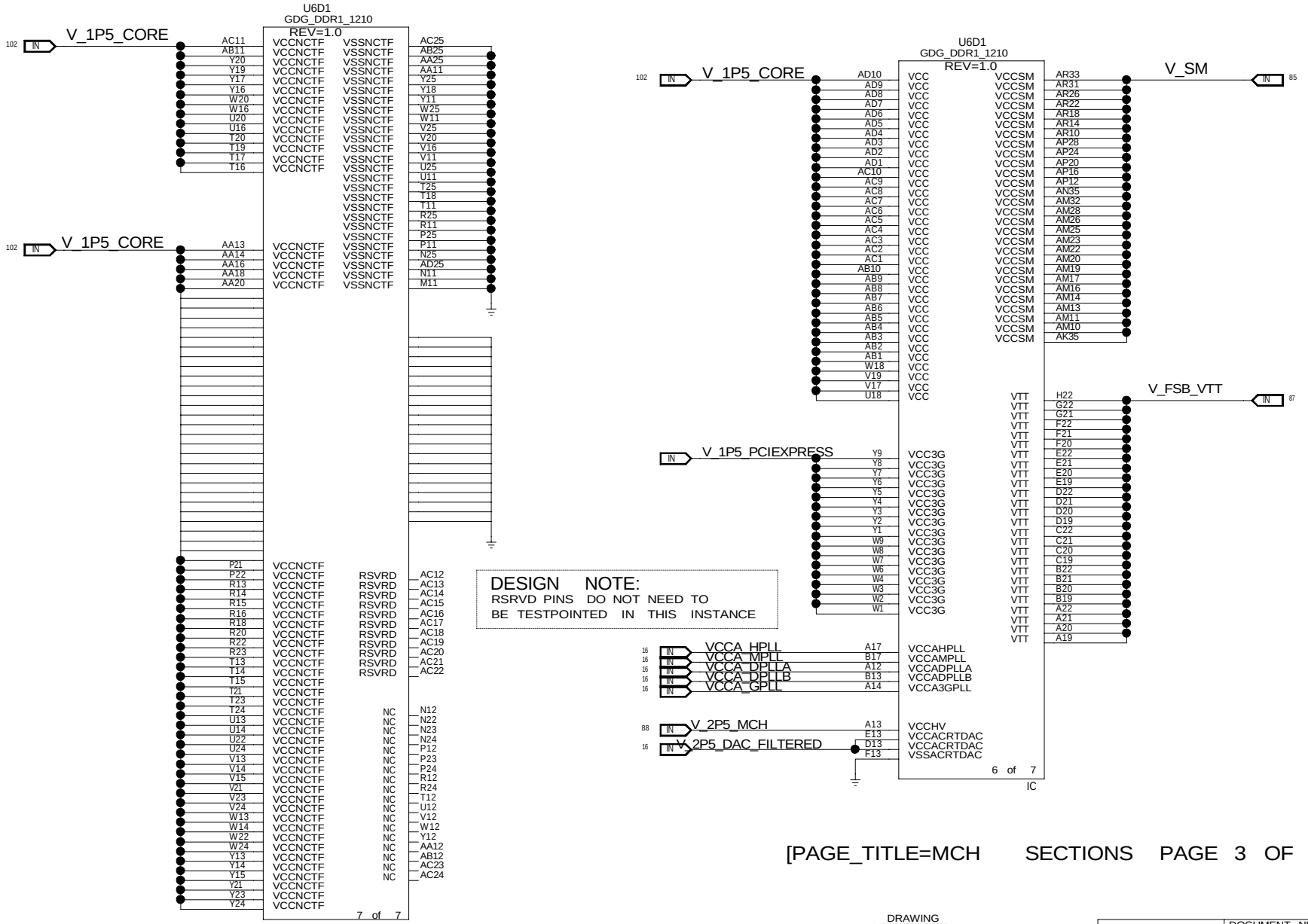
1	SDVO CARD PRESENT, PEG DISABLED
0	SDVO DISABLED (DEFAULT)

[PAGE_TITLE=MCH SECTIONS PAGE 2 OF 6]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.11
Wed Apr 06 22:21:10 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	11	1.00

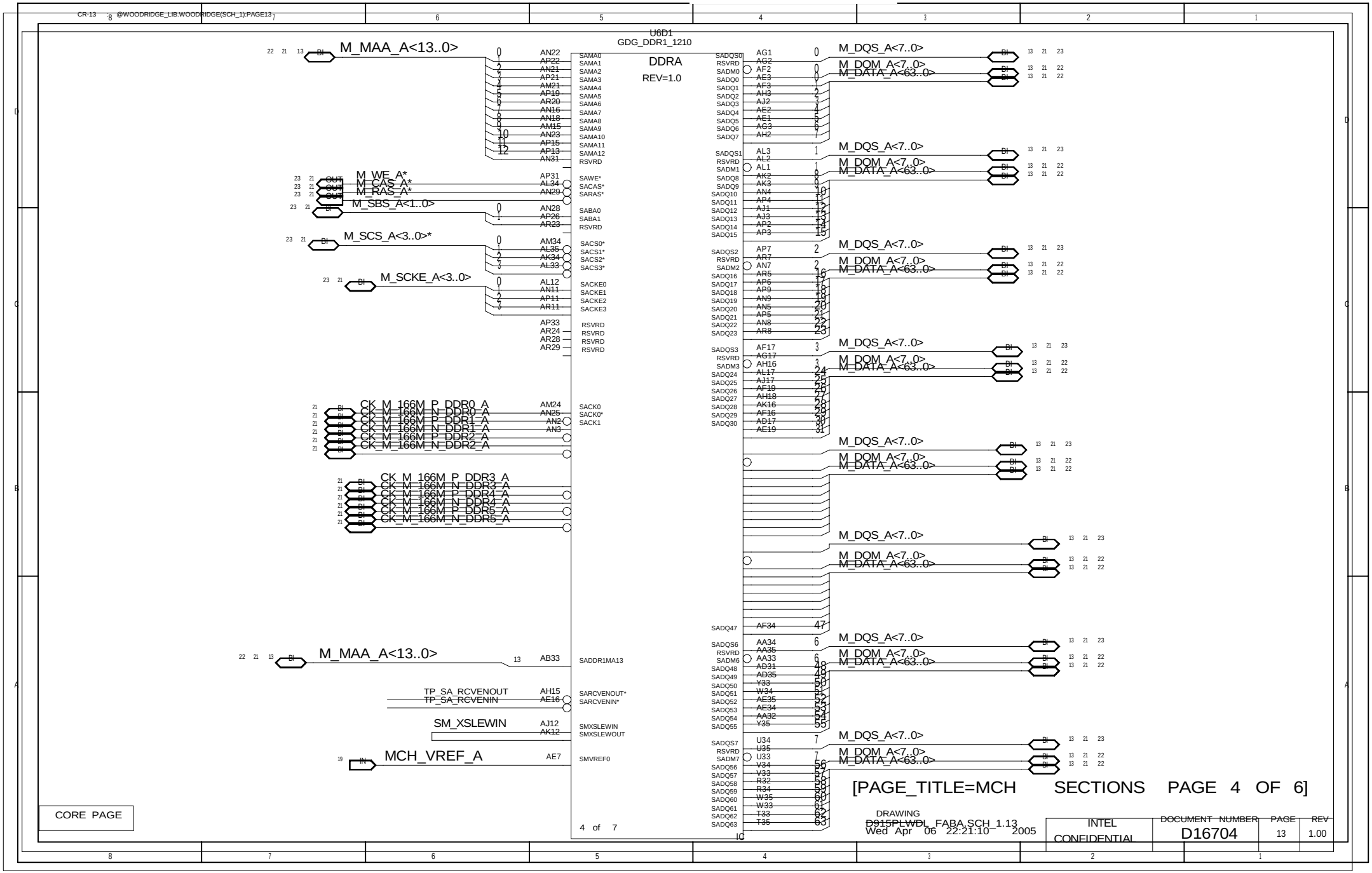


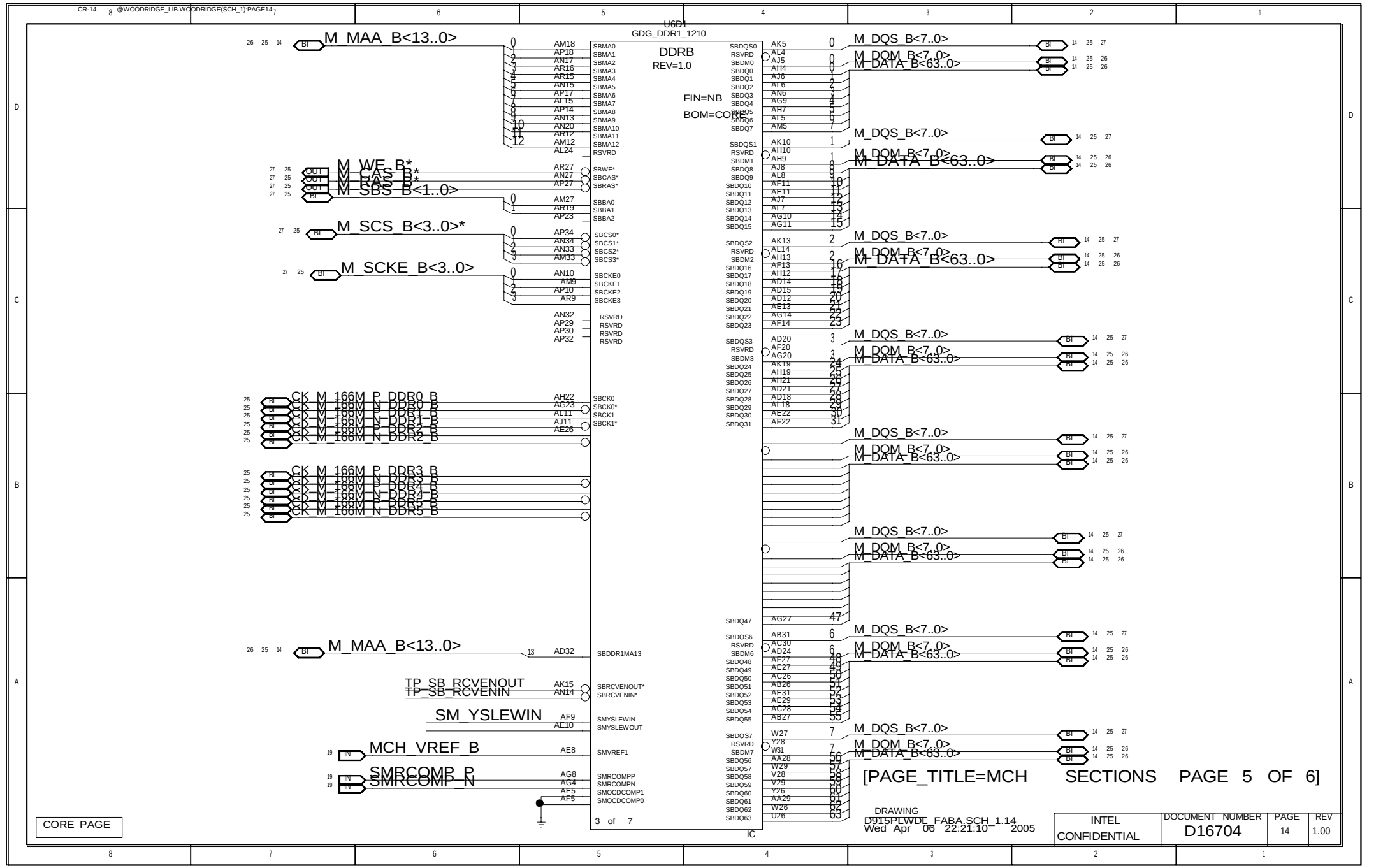
[PAGE_TITLE=MCH SECTIONS PAGE 3 OF 6]

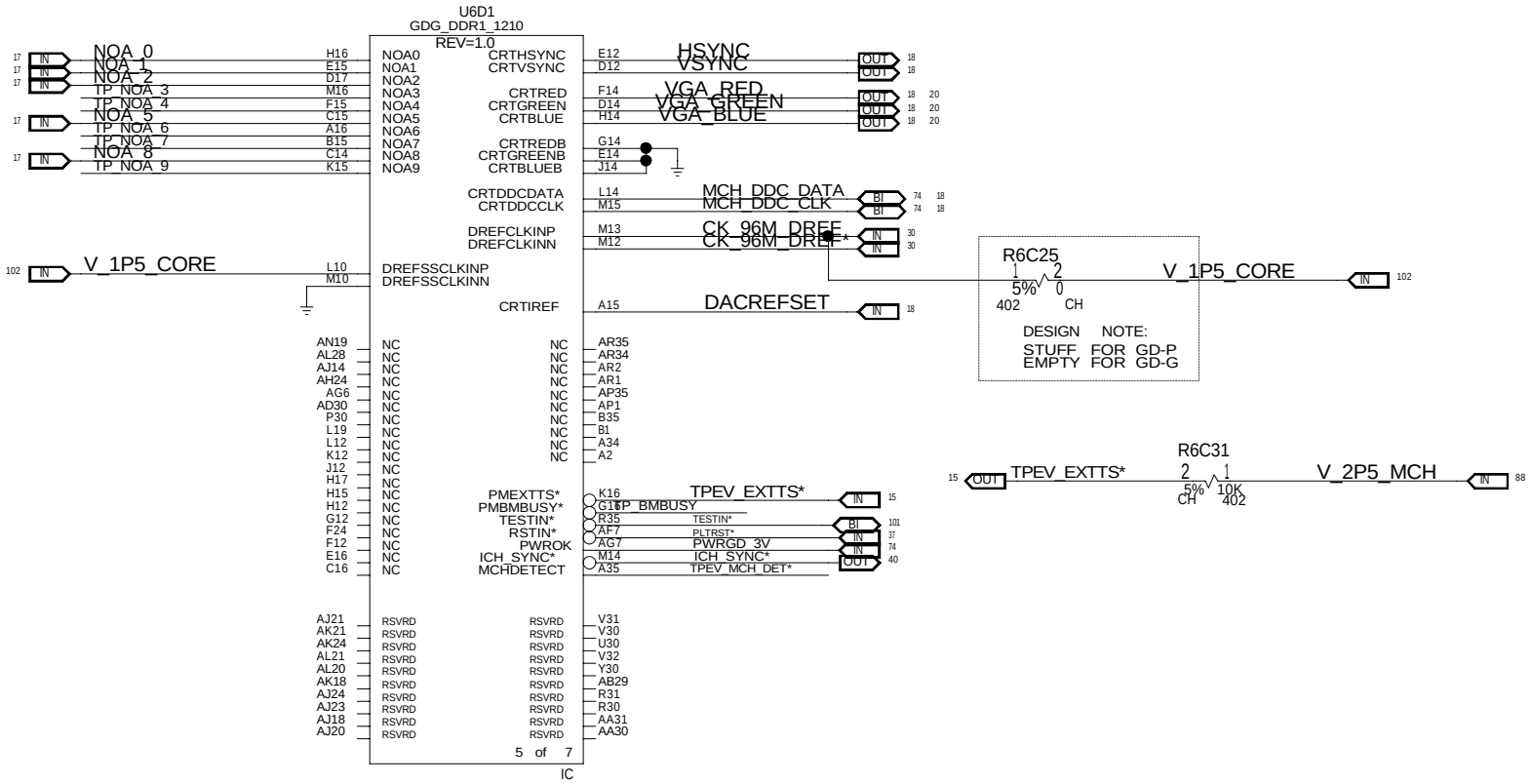
CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.12
Wed Apr 06 22:21:10 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	12	1.00


CR-13
@WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE13
U6D1
GDG_DDR1_1210
DDRA
REV=1.0
M_MAA_A<13..0>
M_WE_A*
M_CAS_A*
M_RAS_A*
M_SBS_A<1..0>
M_SCS_A<3..0>*
M_SCKE_A<3..0>
CK_M_166M_P_DDR0_A
CK_M_166M_N_DDR0_A
CK_M_166M_P_DDR1_A
CK_M_166M_N_DDR1_A
CK_M_166M_P_DDR2_A
CK_M_166M_N_DDR2_A
CK_M_166M_P_DDR3_A
CK_M_166M_N_DDR3_A
CK_M_166M_P_DDR4_A
CK_M_166M_N_DDR4_A
CK_M_166M_P_DDR5_A
CK_M_166M_N_DDR5_A
M_MAA_A<13..0>
TP_SA_RCVENOUT
TP_SA_RCVENIN
SM_XSLEWIN
MCH_VREF_A
M_DQS_A<7..0>
M_DQM_A<7..0>
M_DATA_A<63..0>
4 of 7
IC
[PAGE_TITLE=MCH SECTIONS PAGE 4 OF 6]
CORE PAGE
DRAWING
D915PLWDL_FABA.SCH_1.13
Wed Apr 06 22:21:10 2005
INTEL CONFIDENTIAL
DOCUMENT NUMBER
D16704
PAGE
13
REV
1.00


CR-14 :8 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE14
U6D1
GDG_DDR1_1210
DDRB
REV=1.0
FIN=NB
BOM=CORE
M_MAA_B<13..0>
M_WE_B*
M_CAS_B*
M_RAS_B*
M_SBS_B<1..0>
M_SCS_B<3..0>*
M_SCKE_B<3..0>
CK_M_166M_P_DDR0_B
CK_M_166M_N_DDR0_B
CK_M_166M_P_DDR1_B
CK_M_166M_N_DDR1_B
CK_M_166M_P_DDR2_B
CK_M_166M_N_DDR2_B
CK_M_166M_P_DDR3_B
CK_M_166M_N_DDR3_B
CK_M_166M_P_DDR4_B
CK_M_166M_N_DDR4_B
CK_M_166M_P_DDR5_B
CK_M_166M_N_DDR5_B
M_MAA_B<13..0>
TP_SB_RCVENOUT
TP_SB_RCVENIN
SM_YSLEWIN
MCH_VREF_B
SMRCOMP_P
SMRCOMP_N
M_DQS_B<7..0>
M_DQM_B<7..0>
M_DATA_B<63..0>
3 of 7
IC
[PAGE_TITLE=MCH SECTIONS PAGE 5 OF 6]
DRAWING
D915PLWDL_FABA.SCH_1.14
Wed Apr 06 22:21:10 2005
CORE PAGE
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
D16704
PAGE
14
REV
1.00



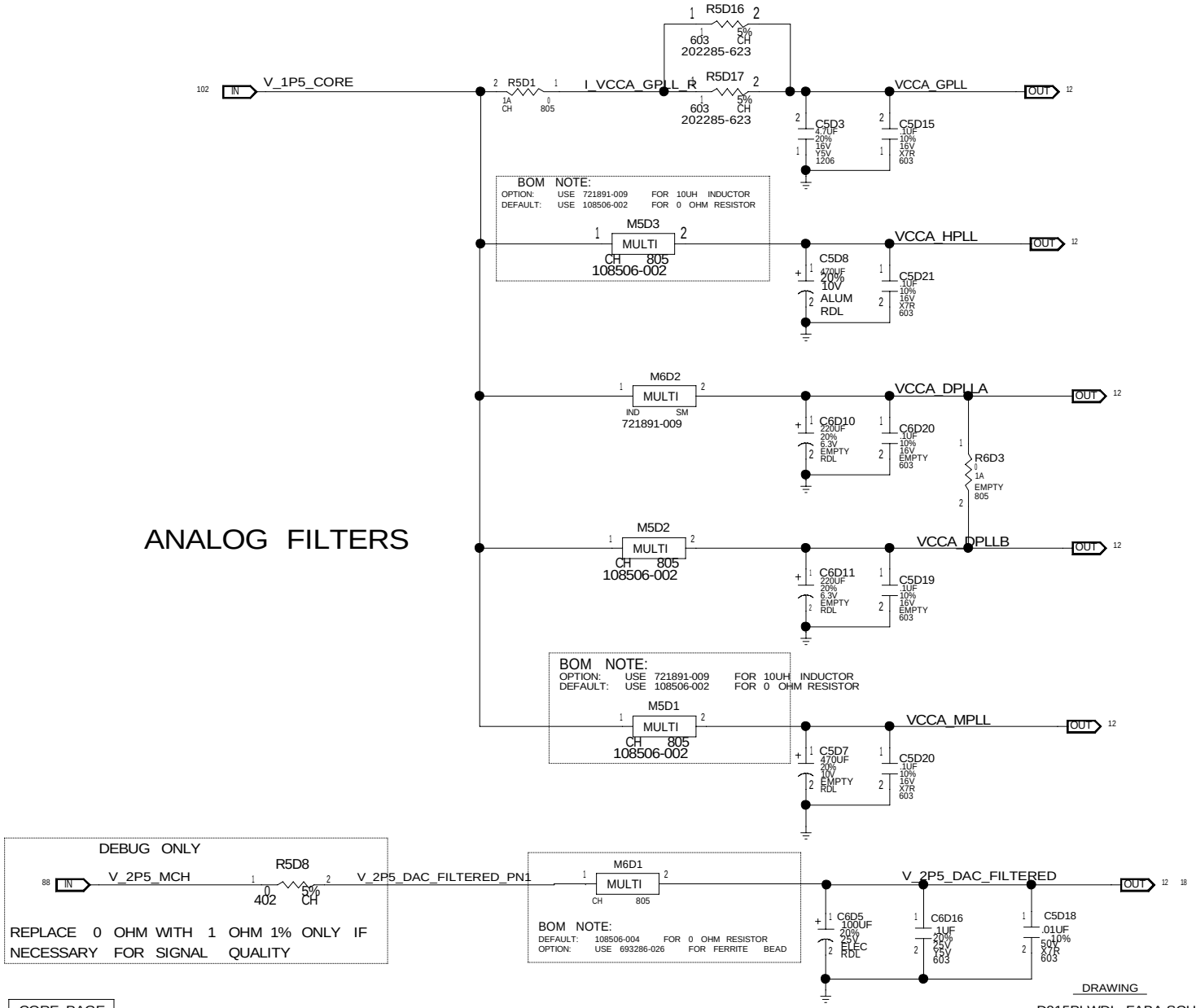
[PAGE_TITLE=MCH SECTIONS PAGE 6 OF 6]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.15
Thu Apr 07 00:59:40 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	15	1.00

ANALOG FILTERS



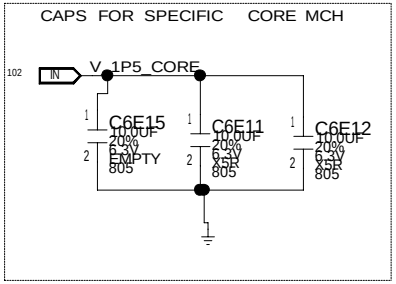
CORE PAGE

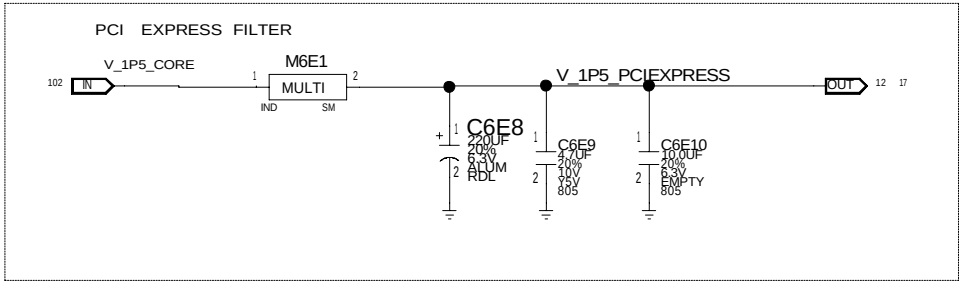
DRAWING

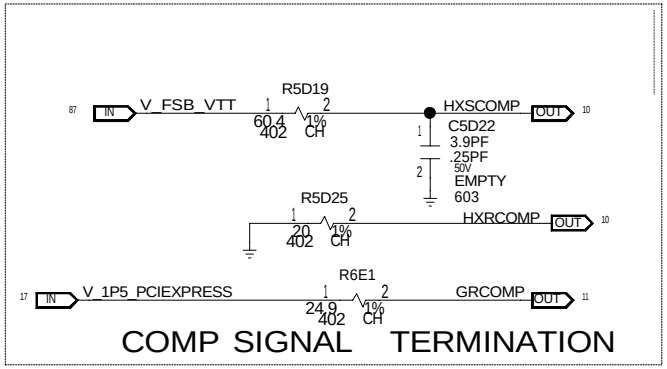
D915PLWDL_FABA.SCH_1.16
Thu Apr 07 00:59:17 2005

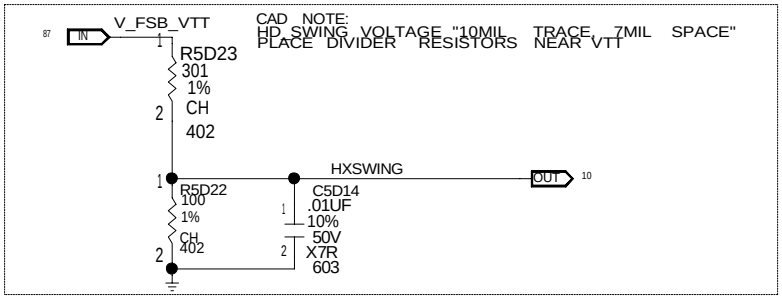
[PAGE_TITLE=MCH 2P5_DAC & 1P5 FILTER]

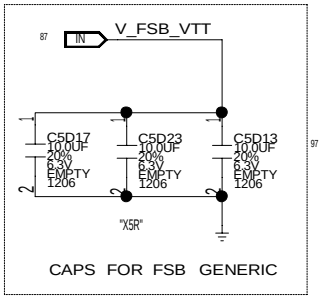
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	16	1.00

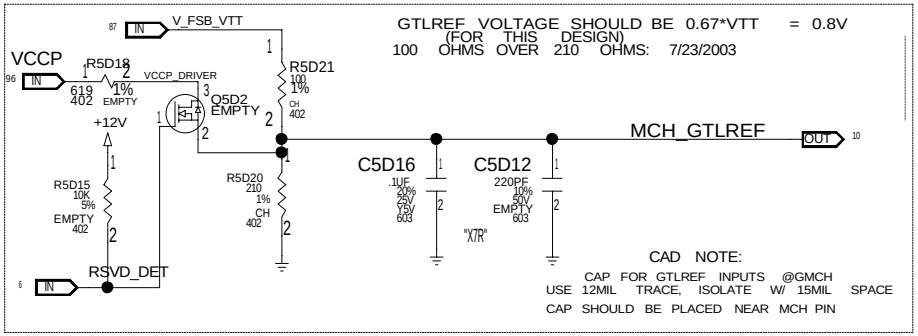




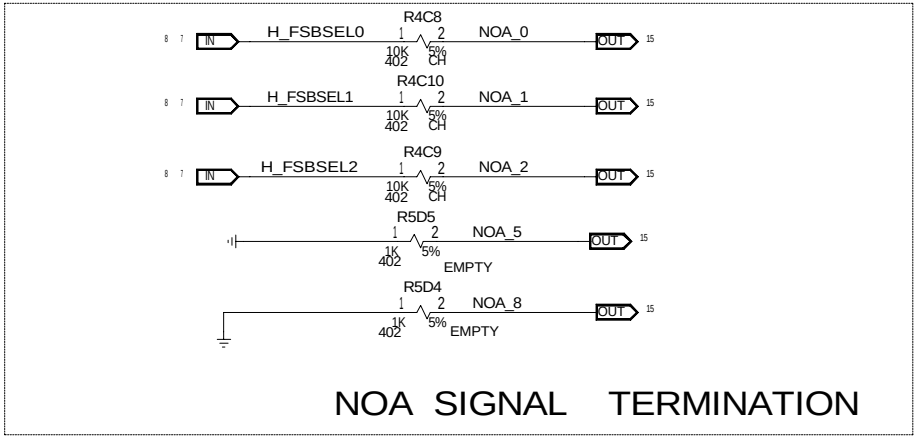








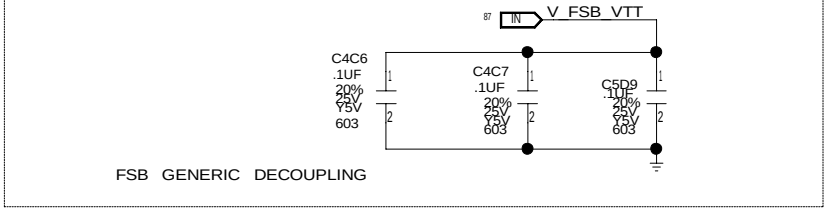
NOA	H	L	DESCRIPTION
0	SEE BSEL TABLE		BSEL0
1	SEE BSEL TABLE		BSEL1
2	SEE BSEL TABLE		BSEL2
3	NORM	ALL-Z	ALL-Z TEST MODE
4	NORM	XOR	XOR CHAIN
5	DDR1	DDR2	MEMORY TYPE
6	NORM	REVERSE	PCI-EXPRESS LANE REVERSAL
7	DIS	ENABLE	FSB HARDWARE STRAPS
8	NEW LTSSM	OLD LTSSM	LTSSM MODE (1.0 OLD, 1.0A NEW)
9	NORM	BYPASS	ICH PCI-EXPRESS RST BYPASS
3,4,5,6,7,8,9	ALL HAVE INTERNAL PULL-UP		



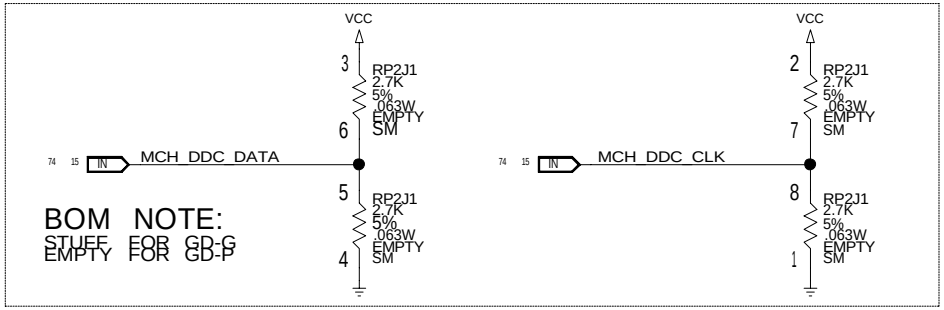
BSEL			PSB FREQUENCY		
2	1	0			
0	0	0	267	MHZ	(1067)
0	0	1	133	MHZ	(533)
0	1	0	200	MHZ	(800)
0	1	1	167	MHZ	(667)
1	0	0	333	MHZ	(RSVD)
1	0	1	100	MHZ	(400)
1	1	0	400	MHZ	(RSVD)
1	1	1	RESERVED		

CORE PAGE

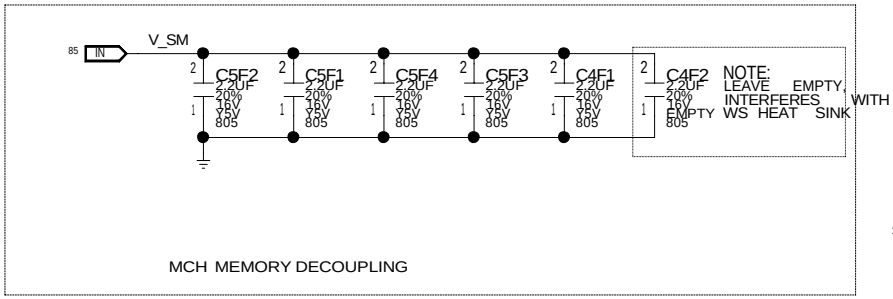
[PAGE_TITLE=MCH DECOUPLING AND COMP]



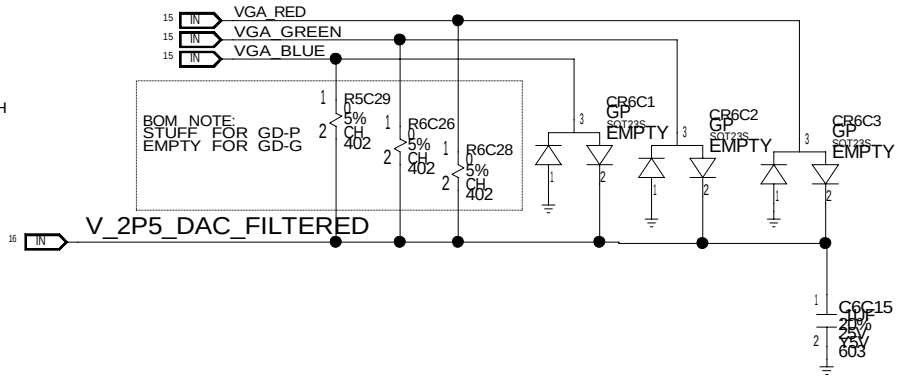
FSB GENERIC DECOUPLING

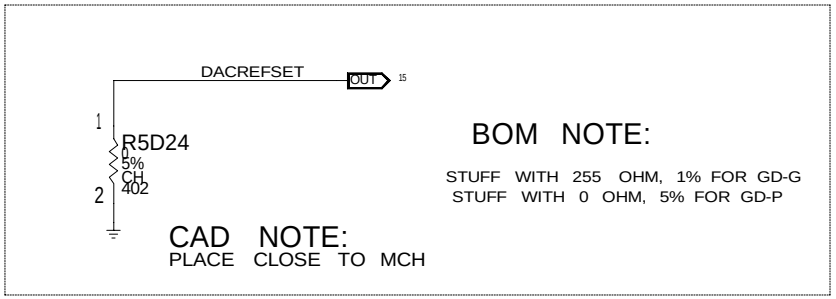


BOM NOTE:
STUFF FOR GD-G
EMPTY FOR GD-P



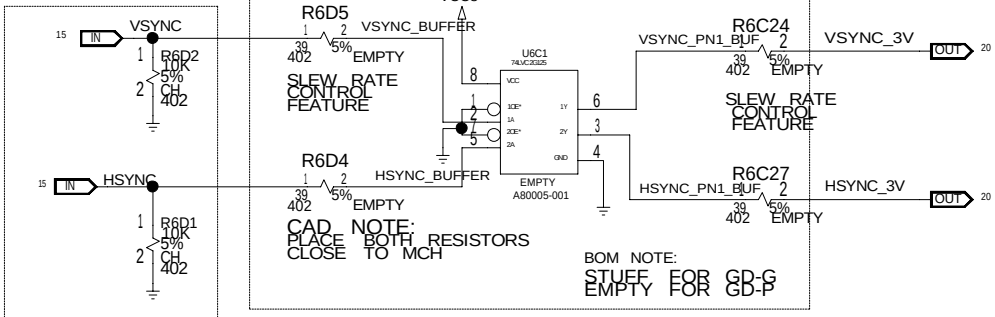
MCH MEMORY DECOUPLING





BOM NOTE:
STUFF WITH 255 OHM, 1% FOR GD-G
STUFF WITH 0 OHM, 5% FOR GD-P

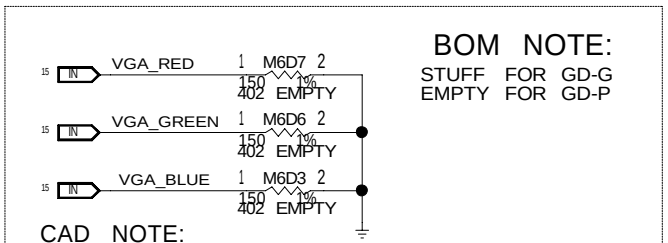
CAD NOTE:
PLACE CLOSE TO MCH



BOM NOTE:
STUFF FOR GD-P
EMPTY FOR GD-G

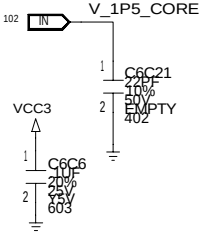
CAD NOTE:
PLACE BOTH RESISTORS CLOSE TO MCH

BOM NOTE:
STUFF FOR GD-G
EMPTY FOR GD-P



CAD NOTE:
PLACE CLOSE TO MCH, WITHIN 750 MIL OF PIN

BOM NOTE:
STUFF FOR GD-G
EMPTY FOR GD-P



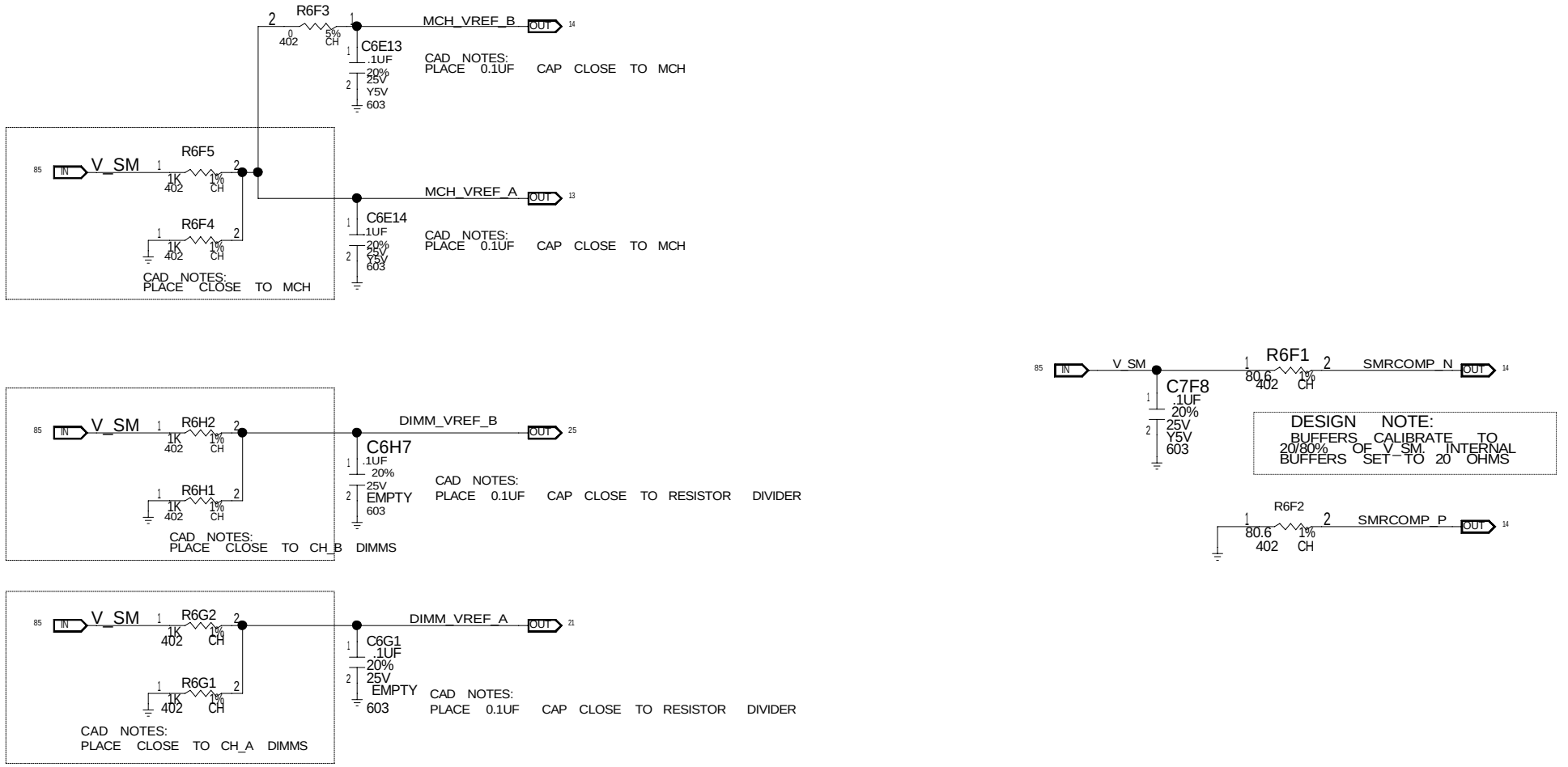
CORE PAGE

DESIGN NOTE:
PER THE SPEC: ALL UNUSED INPUTS OF THE DEVICE MUST BE HELD AT VCC/VCC3 OR GND TO ENSURE PROPER DEVICE OPERATION.
PER THE SPEC: DESIGNED FOR 1.65-V TO 5.5-V VCC OPERATION.

[PAGE_TITLE=MCH DCPL & VGA TERMINATION]

DRAWING
D915PLWDL_FABA.SCH_1.18
Thu Apr 07 00:59:26 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	18	1.00

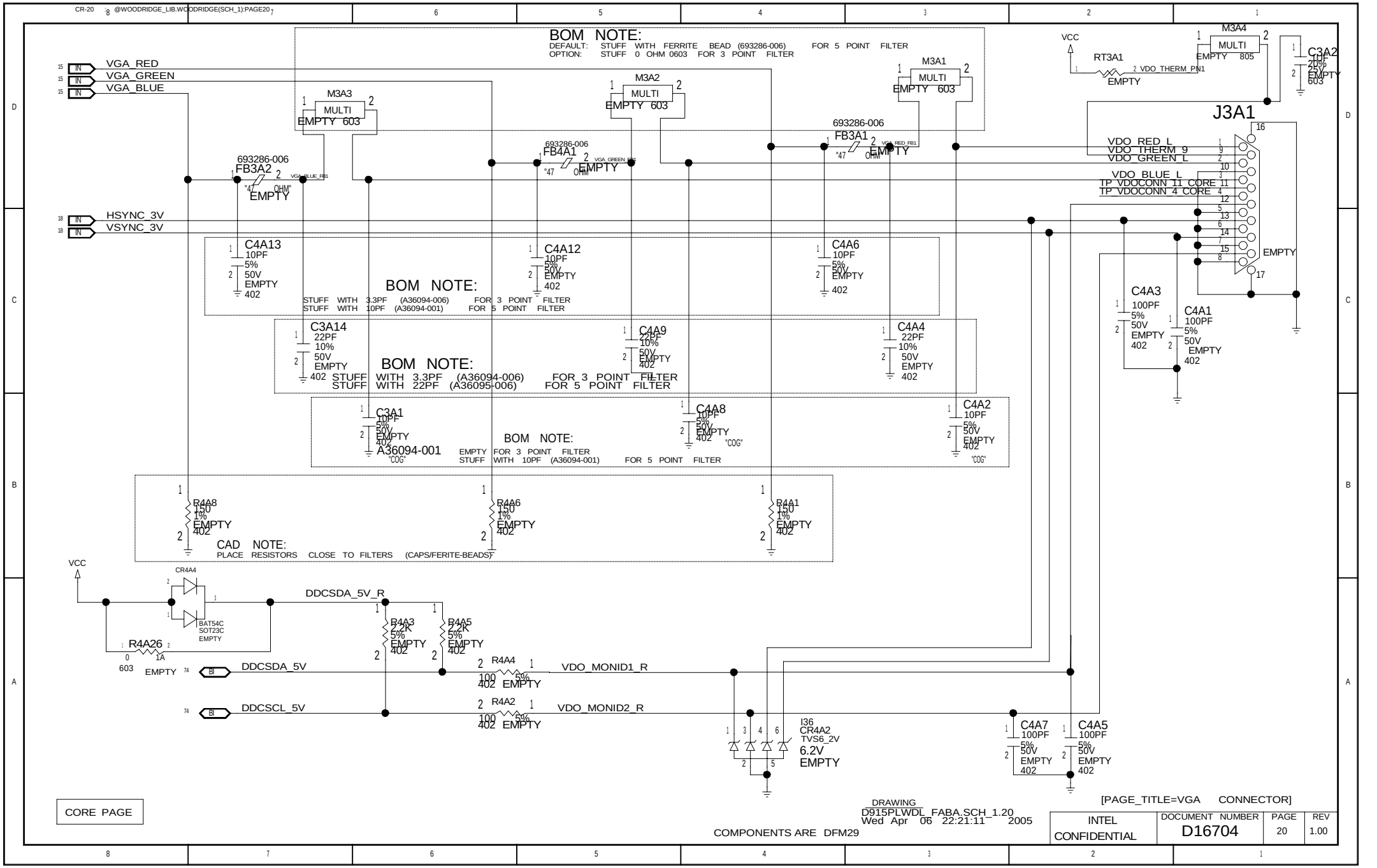


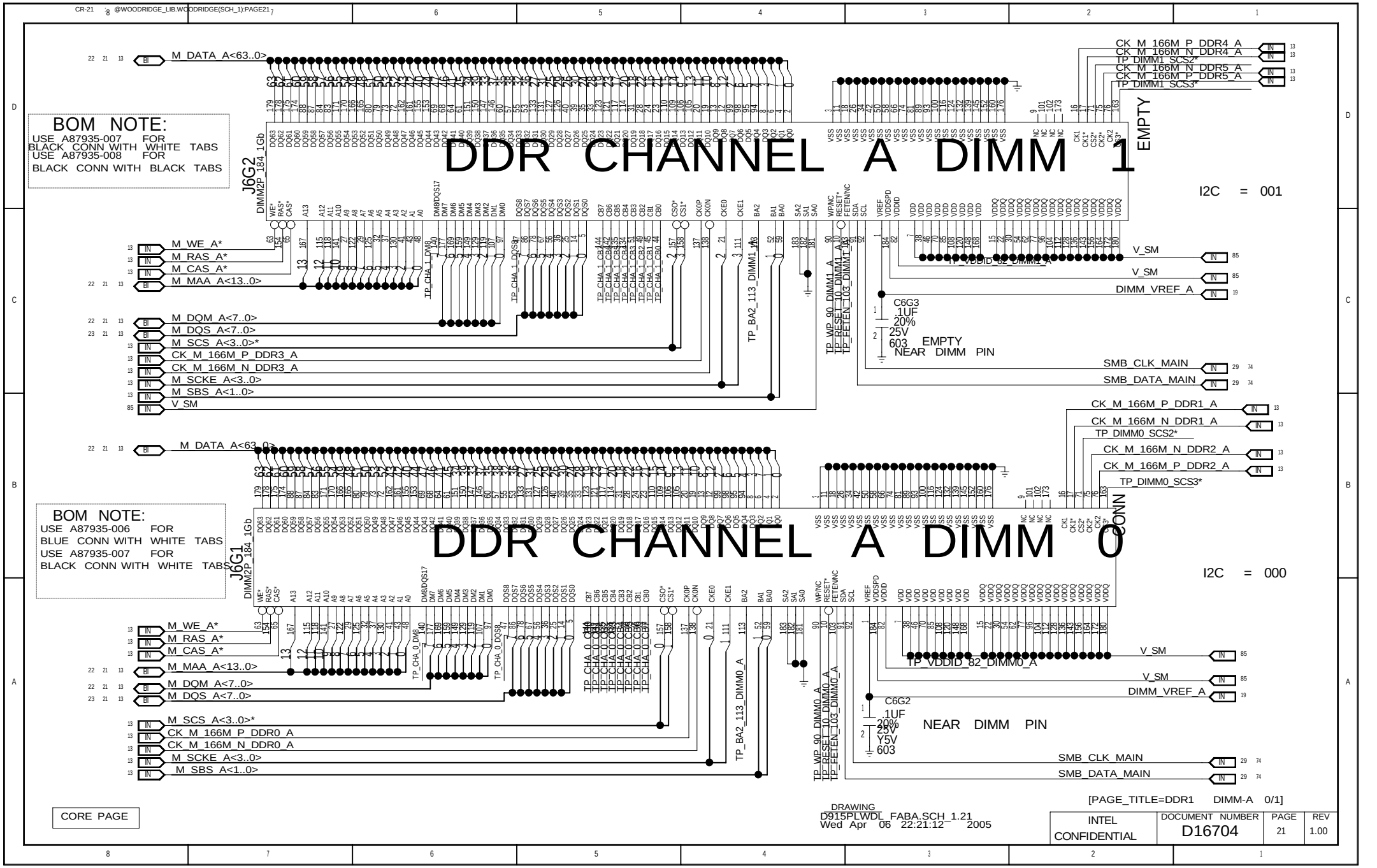
[PAGE_TITLE=MCH CHIPSET TERMINATION]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.19
Thu Apr 07 00:59:31 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	19	1.00


CR-20 :8 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE20
BOM NOTE:
DEFAULT: STUFF WITH FERRITE BEAD (693286-006) FOR 5 POINT FILTER
OPTION: STUFF 0 OHM 0603 FOR 3 POINT FILTER
VGA_RED
VGA_GREEN
VGA_BLUE
HSYNC_3V
VSYNC_3V
M3A3 MULTI EMPTY 603
M3A2 MULTI EMPTY 603
M3A1 MULTI EMPTY 603
M3A4 MULTI EMPTY 805
693286-006 FB3A2 "47 OHM" EMPTY
693286-006 FB4A1 "47 OHM" EMPTY
693286-006 FB3A1 "47 OHM" EMPTY
VGA_BLUE_FB1
VGA_GREEN_FB1
VGA_RED_FB1
VCC
RT3A1 EMPTY
VDO_THERM_PN1
C3A2 10PF 20% 25V EMPTY 603
J3A1
VDO_RED_L
VDO_THERM_9
VDO_GREEN_L
VDO_BLUE_L
TP_VDOCONN_11_CORE
TP_VDOCONN_4_CORE
EMPTY
C4A13 10PF 5% 50V EMPTY 402
C4A12 10PF 5% 50V EMPTY 402
C4A6 10PF 5% 50V EMPTY 402
BOM NOTE:
STUFF WITH 3.3PF (A36094-006) FOR 3 POINT FILTER
STUFF WITH 10PF (A36094-001) FOR 5 POINT FILTER
C3A14 22PF 10% 50V EMPTY 402
C4A9 22PF 10% 50V EMPTY 402
C4A4 22PF 10% 50V EMPTY 402
BOM NOTE:
STUFF WITH 3.3PF (A36094-006) FOR 3 POINT FILTER
STUFF WITH 22PF (A36095-006) FOR 5 POINT FILTER
C3A1 10PF 5% 50V EMPTY 402 A36094-001 "COG"
C4A8 10PF 5% 50V EMPTY 402 "COG"
C4A2 10PF 5% 50V EMPTY 402 "COG"
BOM NOTE:
EMPTY FOR 3 POINT FILTER
STUFF WITH 10PF (A36094-001) FOR 5 POINT FILTER
C4A3 100PF 5% 50V EMPTY 402
C4A1 100PF 5% 50V EMPTY 402
R4A8 150 1% EMPTY 402
R4A6 150 1% EMPTY 402
R4A1 150 1% EMPTY 402
CAD NOTE:
PLACE RESISTORS CLOSE TO FILTERS (CAPS/FERITE-BEADS)
VCC
CR4A4 BAT54C SOT23C EMPTY
DDCSDA_5V_R
R4A26 0 1A 603 EMPTY
R4A3 2.2K 5% EMPTY 402
R4A5 2.2K 5% EMPTY 402
DDCSDA_5V
DDCSCL_5V
R4A4 100 5% 402 EMPTY
R4A2 100 5% 402 EMPTY
VDO_MONID1_R
VDO_MONID2_R
I36 CR4A2 TVS6_2V 6.2V EMPTY
C4A7 100PF 5% 50V EMPTY 402
C4A5 100PF 5% 50V EMPTY 402
CORE PAGE
DRAWING D915PLWDL_FABA.SCH_1.20 Wed Apr 06 22:21:11 2005
COMPONENTS ARE DFM29
[PAGE_TITLE=VGA CONNECTOR]
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 20
REV 1.00


DDR CHANNEL A DIMM 1
EMPTY
I2C = 001
J6G2
DIMM2P_184_1Gb
BOM NOTE:
USE A87935-007 FOR
BLACK CONN WITH WHITE TABS
USE A87935-008 FOR
BLACK CONN WITH BLACK TABS
M_DATA_A<63..0>
M_WE_A*
M_RAS_A*
M_CAS_A*
M_MAA_A<13..0>
M_DQM_A<7..0>
M_DQS_A<7..0>
M_SCS_A<3..0>*
CK_M_166M_P_DDR3_A
CK_M_166M_N_DDR3_A
M_SCKE_A<3..0>
M_SBS_A<1..0>
V_SM
CK_M_166M_P_DDR4_A
CK_M_166M_N_DDR4_A
TP_DIMM1_SCS2*
CK_M_166M_N_DDR5_A
CK_M_166M_P_DDR5_A
TP_DIMM1_SCS3*
TP_VDDID_82_DIMM1_A
DIMM_VREF_A
C6G3
.1UF
20%
25V
603
NEAR DIMM PIN
SMB_CLK_MAIN
SMB_DATA_MAIN
TP_WP_90_DIMM1_A
TP_RESET*_10_DIMM1_A
TP_FETEN*_103_DIMM1_A
TP_BA2_113_DIMM1_A
DDR CHANNEL A DIMM 0
CONN
I2C = 000
J6G1
DIMM2P_184_1Gb
BOM NOTE:
USE A87935-006 FOR
BLUE CONN WITH WHITE TABS
USE A87935-007 FOR
BLACK CONN WITH WHITE TABS
M_DATA_A<63..0>
M_WE_A*
M_RAS_A*
M_CAS_A*
M_MAA_A<13..0>
M_DQM_A<7..0>
M_DQS_A<7..0>
M_SCS_A<3..0>*
CK_M_166M_P_DDR0_A
CK_M_166M_N_DDR0_A
M_SCKE_A<3..0>
M_SBS_A<1..0>
CK_M_166M_P_DDR1_A
CK_M_166M_N_DDR1_A
TP_DIMM0_SCS2*
CK_M_166M_N_DDR2_A
CK_M_166M_P_DDR2_A
TP_DIMM0_SCS3*
TP_VDDID_82_DIMM0_A
DIMM_VREF_A
C6G2
.1UF
20%
25V
Y5V
603
NEAR DIMM PIN
SMB_CLK_MAIN
SMB_DATA_MAIN
TP_WP_90_DIMM0_A
TP_RESET*_10_DIMM0_A
TP_FETEN*_103_DIMM0_A
TP_BA2_113_DIMM0_A
CORE PAGE
DRAWING
D915PLWDL_FABA.SCH_1.21
Wed Apr 06 22:21:12 2005
[PAGE_TITLE=DDR1 DIMM-A 0/1]
INTEL CONFIDENTIAL
DOCUMENT NUMBER
D16704
PAGE
21
REV
1.00

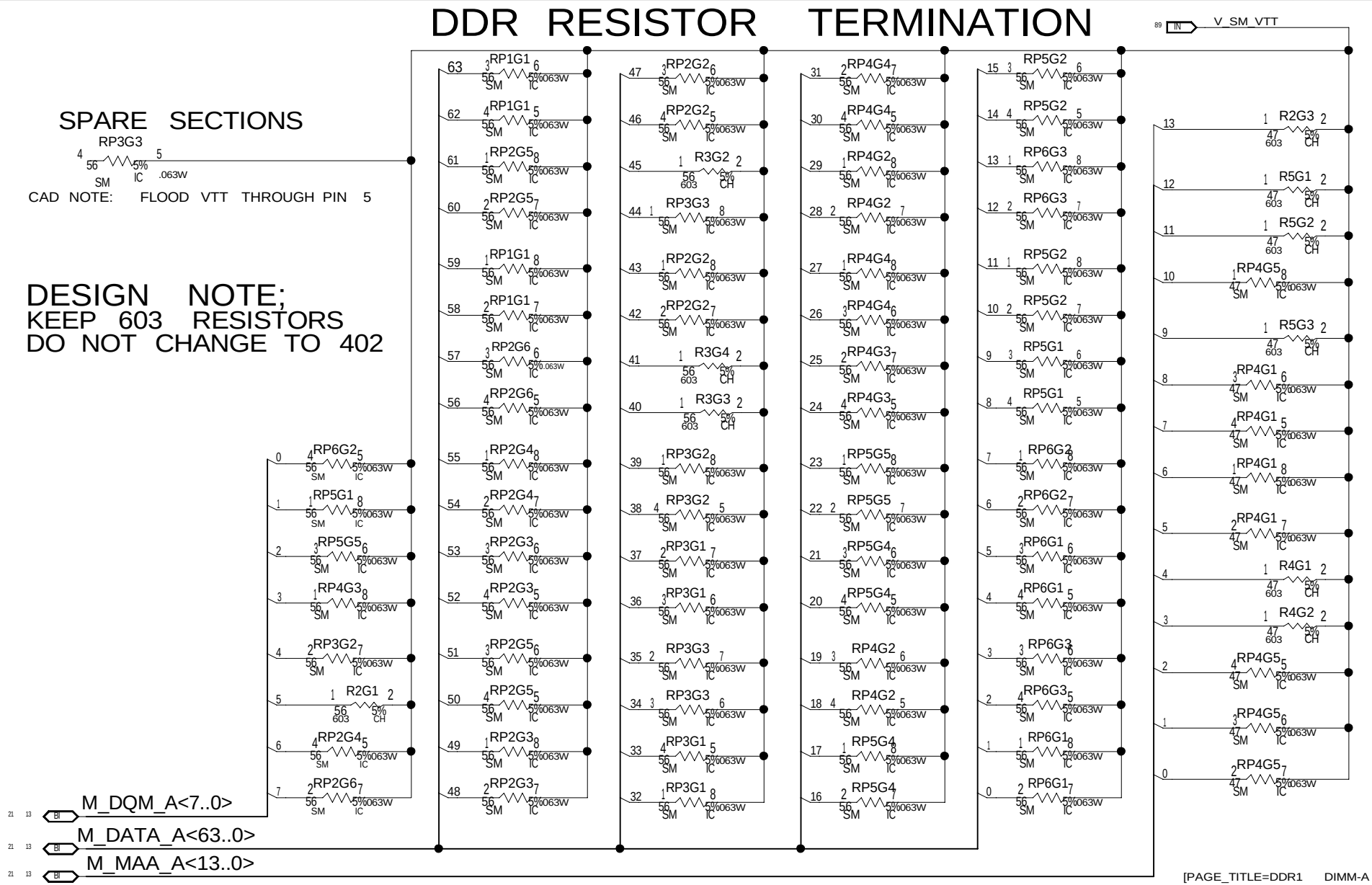
DDR RESISTOR TERMINATION

SPARE SECTIONS

RP3G3 4 56 SM 5% IC .063W 5

CAD NOTE: FLOOD VTT THROUGH PIN 5

DESIGN NOTE;
KEEP 603 RESISTORS
DO NOT CHANGE TO 402



[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM]

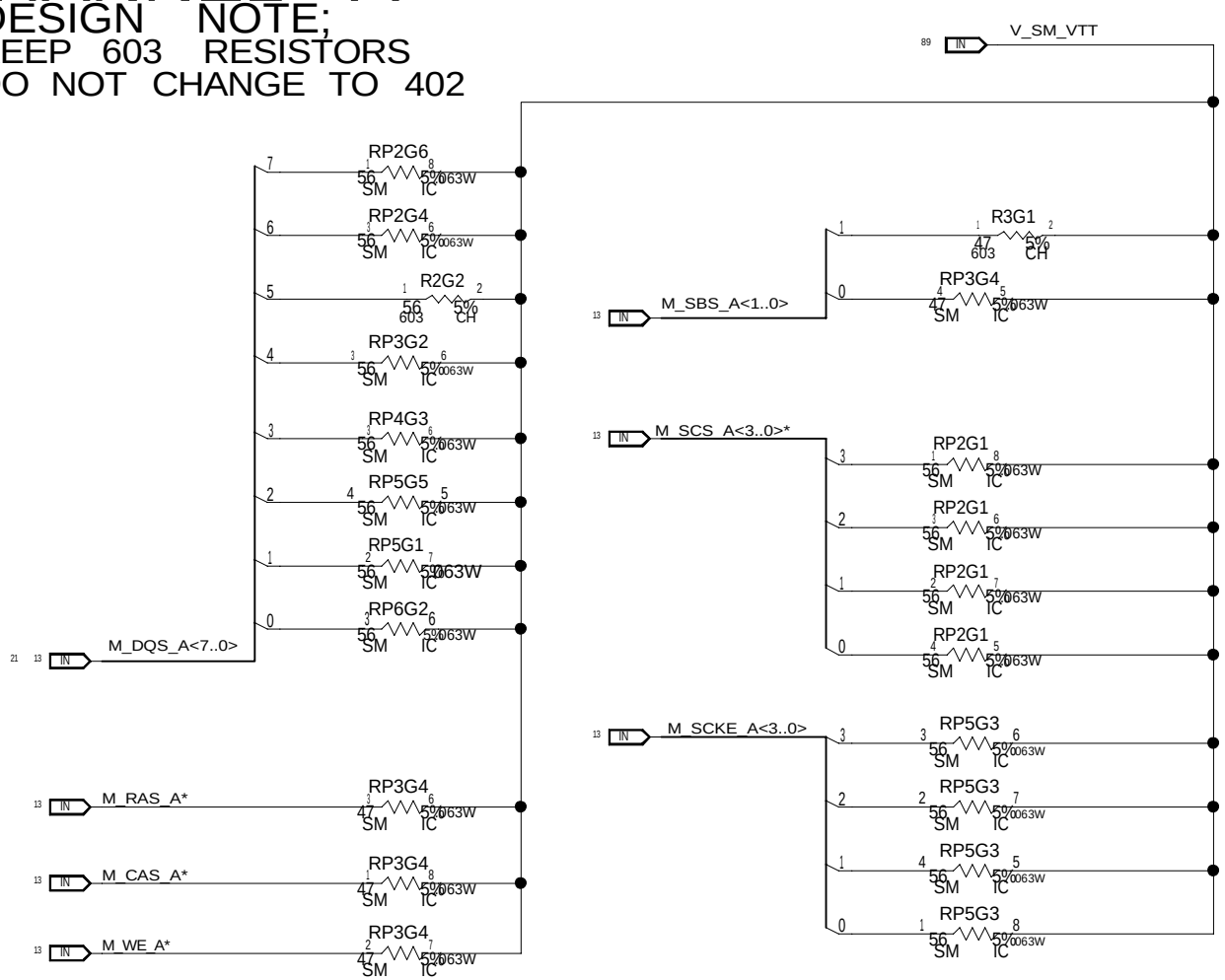
CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.22
Wed Apr 06 22:21:12 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	22	1.00

CHANNEL A

DESIGN NOTE;
KEEP 603 RESISTORS
DO NOT CHANGE TO 402



DDR RESISTOR TERMINATION

CORE PAGE

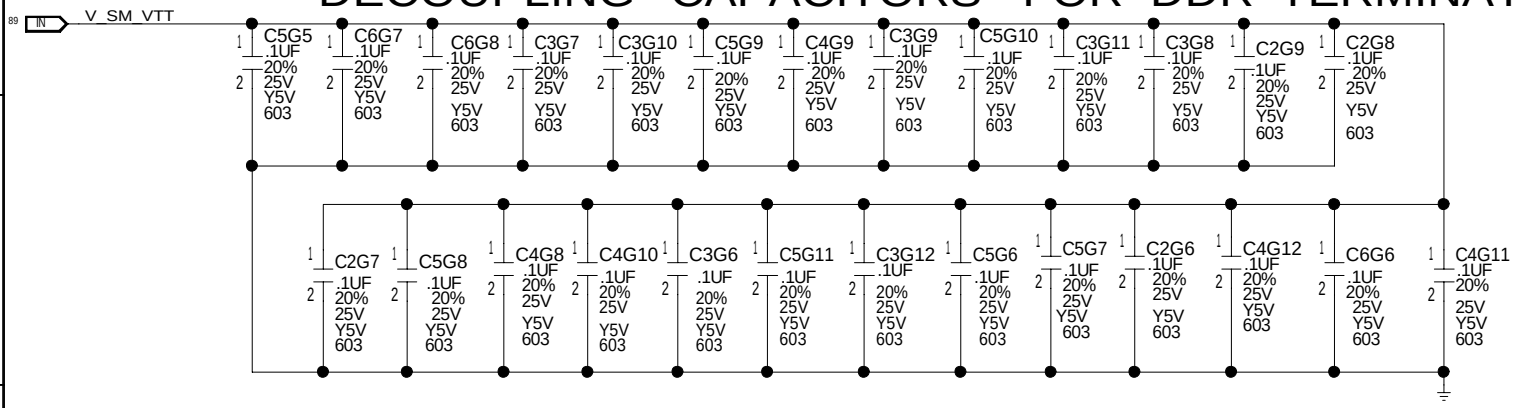
[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM]

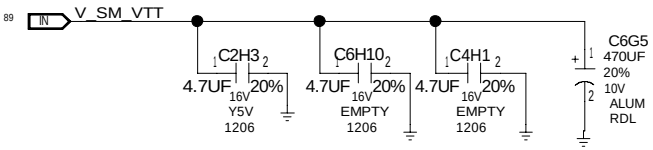
DRAWING
D915PLWDL_FABA.SCH_1.23
Wed Apr 06 22:21:12 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	23	1.00

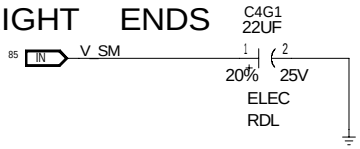
DDR CHANNEL A

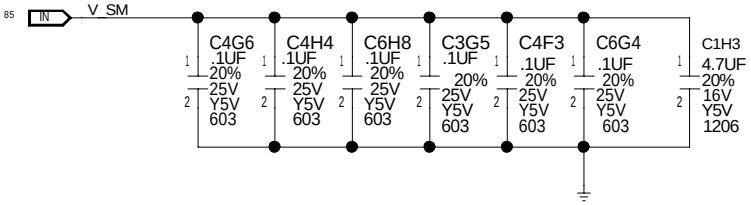
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

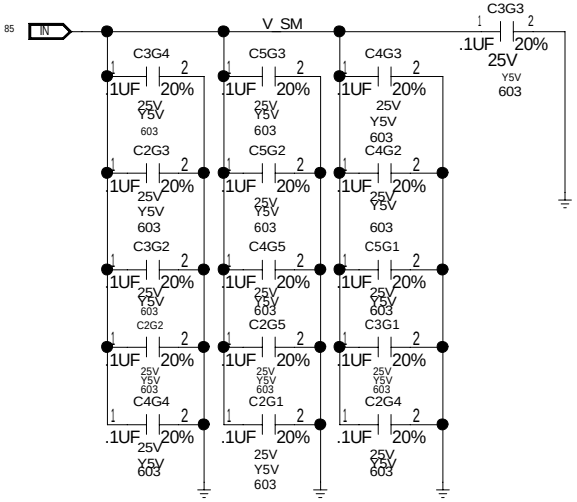




PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND







CHANNEL A
DIMM TO MCH BIT SWAPPING

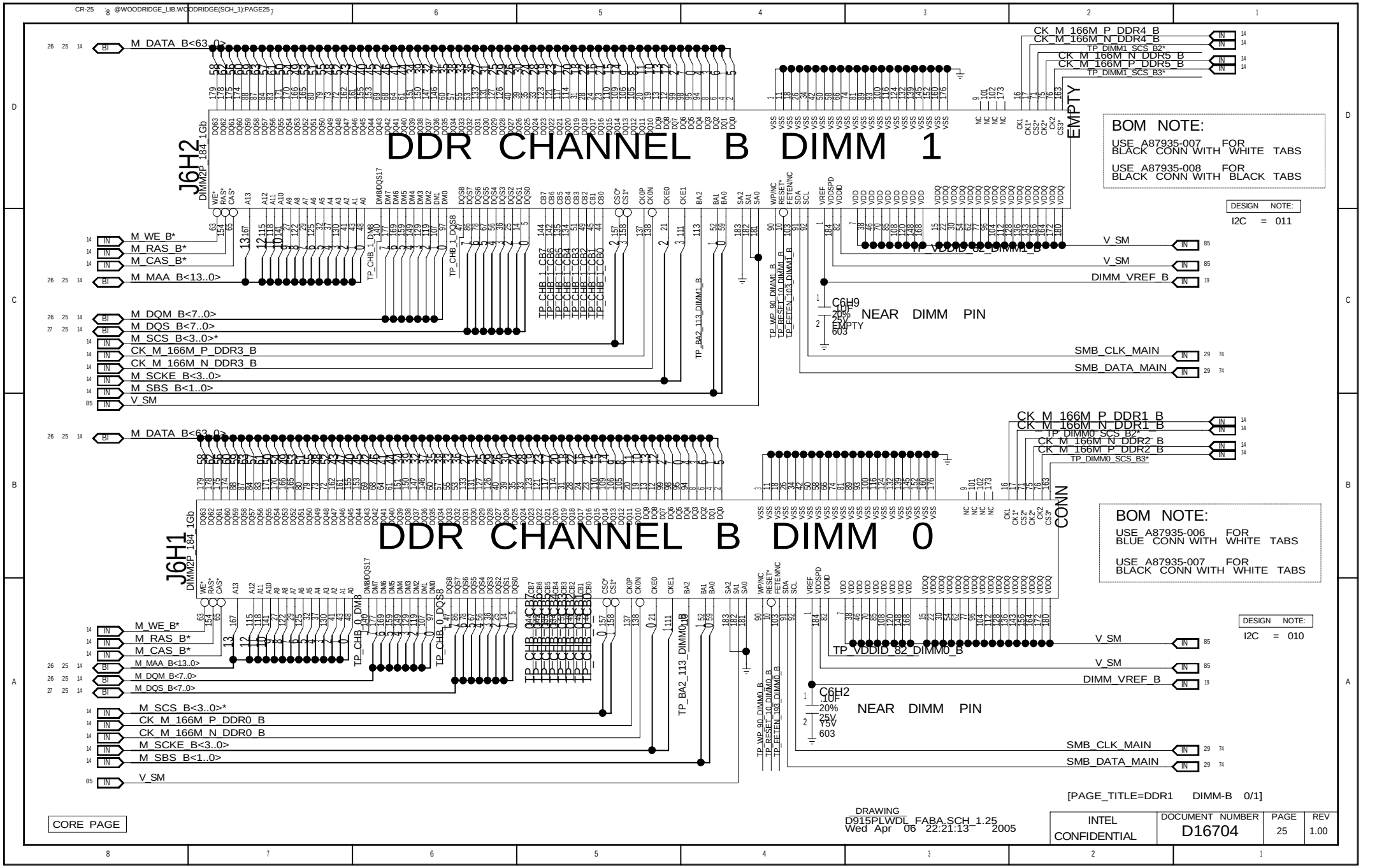
DIMM	MCH
DQ0	DQ0
DQ1	DQ1
DQ2	DQ2
DQ3	DQ3
DQ4	DQ4
DQ5	DQ5
DQ6	DQ6
DQ7	DQ7
DQ8	DQ13
DQ9	DQ9
DQ10	DQ10
DQ11	DQ11
DQ12	DQ12
DQ13	DQ8
DQ14	DQ14
DQ15	DQ15
DQ16	DQ21
DQ17	DQ16
DQ18	DQ22
DQ19	DQ18
DQ20	DQ20
DQ21	DQ17
DQ22	DQ23
DQ23	DQ19
DQ24	DQ28
DQ25	DQ24
DQ26	DQ30
DQ27	DQ26
DQ28	DQ29
DQ29	DQ25
DQ30	DQ31
DQ31	DQ27

DIMM	MCH
DQ32	DQ36
DQ33	DQ32
DQ34	DQ38
DQ35	DQ35
DQ36	DQ37
DQ37	DQ33
DQ38	DQ39
DQ39	DQ34
DQ40	DQ45
DQ41	DQ41
DQ42	DQ46
DQ43	DQ47
DQ44	DQ44
DQ45	DQ40
DQ46	DQ42
DQ47	DQ43
DQ48	DQ52
DQ49	DQ53
DQ50	DQ50
DQ51	DQ51
DQ52	DQ48
DQ53	DQ49
DQ54	DQ54
DQ55	DQ55
DQ56	DQ56
DQ57	DQ57
DQ58	DQ58
DQ59	DQ59
DQ60	DQ60
DQ61	DQ61
DQ62	DQ62
DQ63	DQ63

[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM DCPL]

CORE PAGE

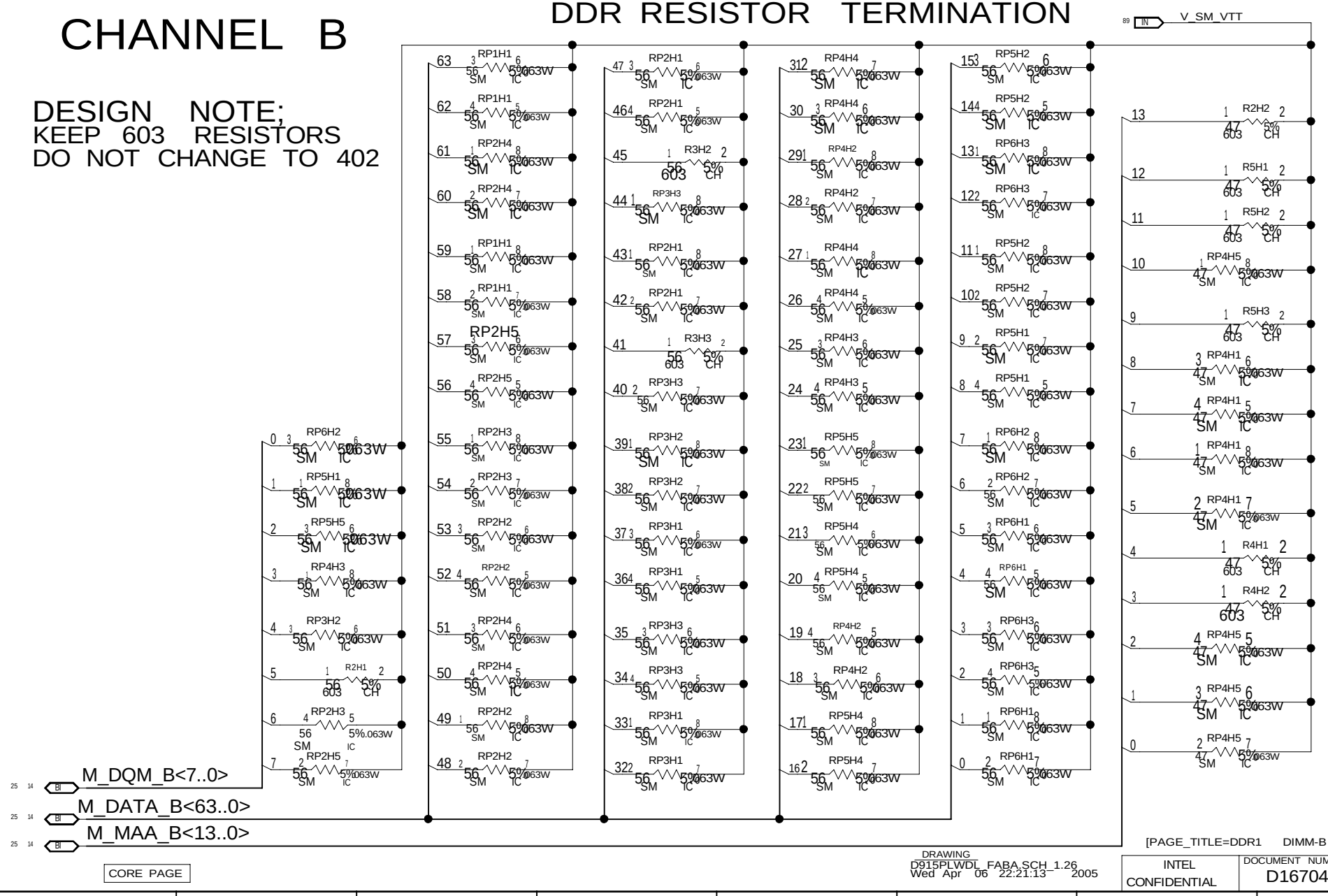
DRAWING
D915PLWDL_FABA.SCH_1.24
Wed Apr 06 22:21:12 2005


DDR CHANNEL B DIMM 1
J6H2
DIMM2P_184_1Gb
EMPTY
BOM NOTE:
USE_A87935-007 FOR BLACK CONN WITH WHITE TABS
USE_A87935-008 FOR BLACK CONN WITH BLACK TABS
DESIGN NOTE:
I2C = 011
M_DATA_B<63..0>
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B<13..0>
M_DQM_B<7..0>
M_DQS_B<7..0>
M_SCS_B<3..0>*
CK_M_166M_P_DDR3_B
CK_M_166M_N_DDR3_B
M_SCKE_B<3..0>
M_SBS_B<1..0>
V_SM
CK_M_166M_P_DDR4_B
CK_M_166M_N_DDR4_B
TP_DIMM1_SCS_B2*
CK_M_166M_N_DDR5_B
CK_M_166M_P_DDR5_B
TP_DIMM1_SCS_B3*
TP_VDDID_82_DIMM1_B
DIMM_VREF_B
C6H9
.1UF
20%
25V
603
NEAR DIMM PIN
SMB_CLK_MAIN
SMB_DATA_MAIN
DDR CHANNEL B DIMM 0
J6H1
DIMM2P_184_1Gb
CONN
BOM NOTE:
USE_A87935-006 FOR BLUE CONN WITH WHITE TABS
USE_A87935-007 FOR BLACK CONN WITH WHITE TABS
DESIGN NOTE:
I2C = 010
M_DATA_B<63..0>
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B<13..0>
M_DQM_B<7..0>
M_DQS_B<7..0>
M_SCS_B<3..0>*
CK_M_166M_P_DDR0_B
CK_M_166M_N_DDR0_B
M_SCKE_B<3..0>
M_SBS_B<1..0>
V_SM
CK_M_166M_P_DDR1_B
CK_M_166M_N_DDR1_B
TP_DIMM0_SCS_B2*
CK_M_166M_N_DDR2_B
CK_M_166M_P_DDR2_B
TP_DIMM0_SCS_B3*
TP_VDDID_82_DIMM0_B
DIMM_VREF_B
C6H2
.1UF
20%
25V
603
NEAR DIMM PIN
SMB_CLK_MAIN
SMB_DATA_MAIN
[PAGE_TITLE=DDR1 DIMM-B 0/1]
CORE PAGE
DRAWING
D915PLWDL_FABA_SCH_1.25
Wed Apr 06 22:21:13 2005
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 25
REV 1.00

CHANNEL B

DDR RESISTOR TERMINATION

DESIGN NOTE;
KEEP 603 RESISTORS
DO NOT CHANGE TO 402



[PAGE_TITLE=DDR1 DIMM-B 0/1 TERM]

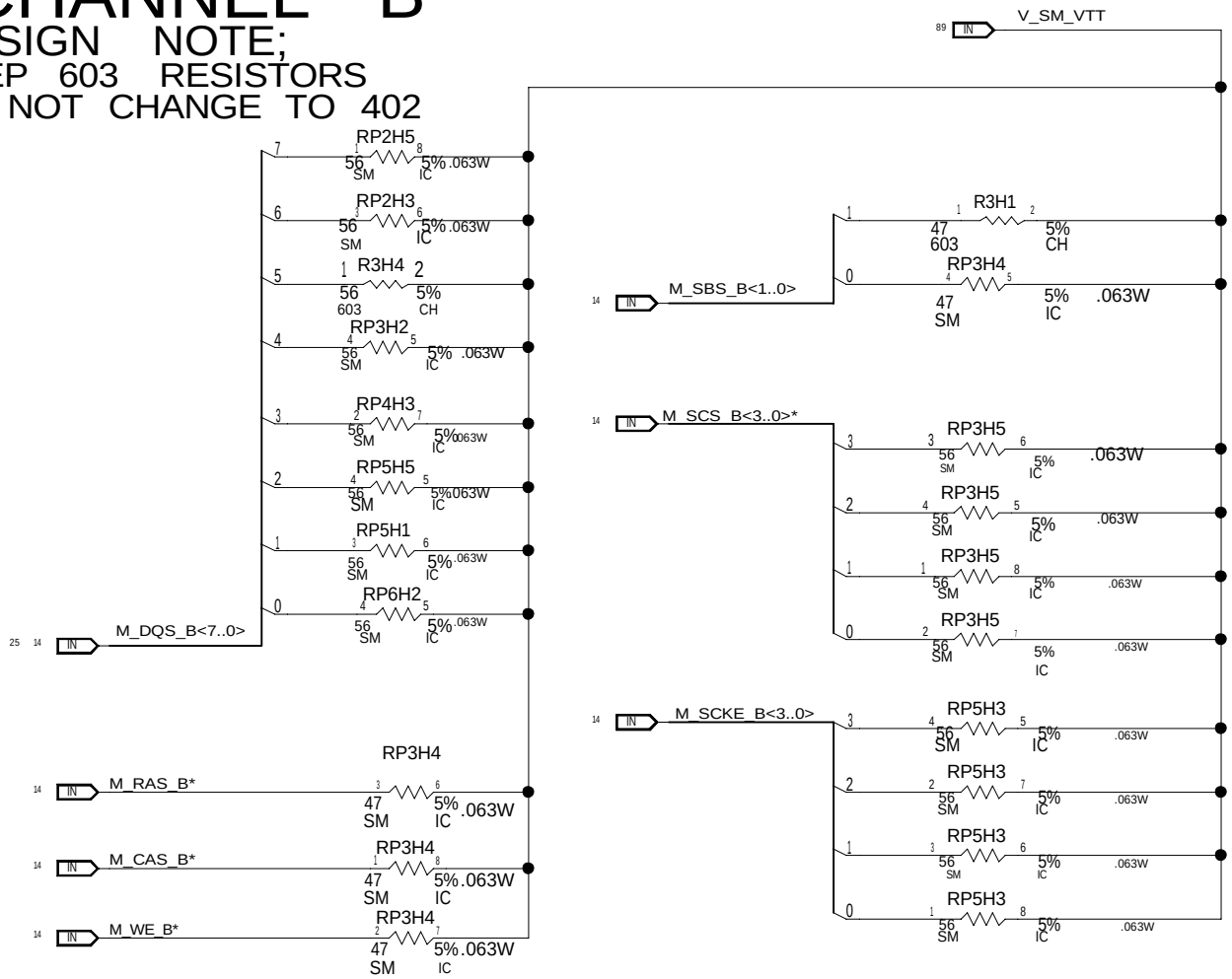
CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.26
Wed Apr 06 22:21:13 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	26	1.00

CHANNEL B

DESIGN NOTE;
KEEP 603 RESISTORS
DO NOT CHANGE TO 402



DDR RESISTOR TERMINATION

[PAGE_TITLE=DDR1 DIMM-B 0/1 TERM]

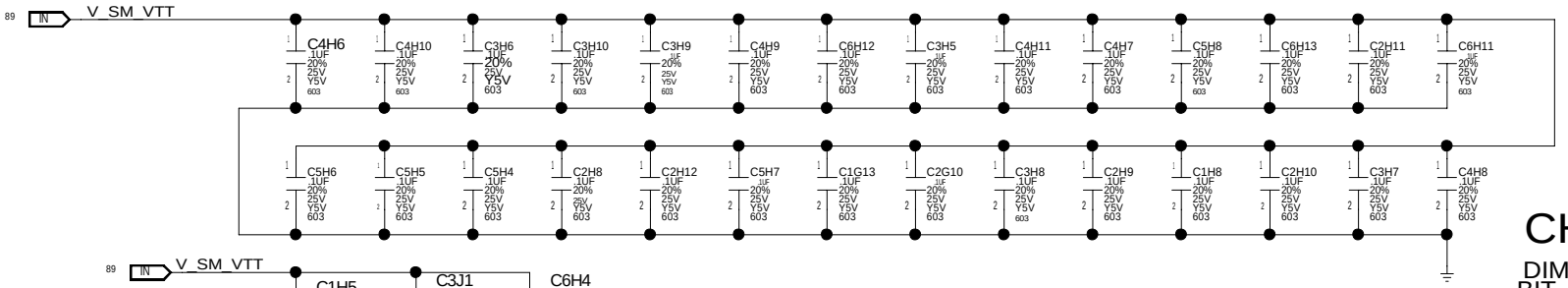
CORE PAGE

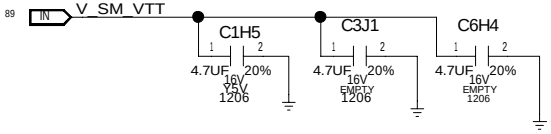
DRAWING
D915PLWDL_FABA.SCH_1.27
Wed Apr 06 22:21:14 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	27	1.00

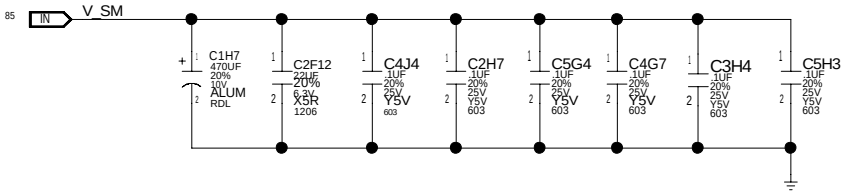
DDR CHANNEL B

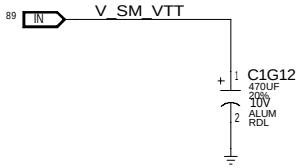
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

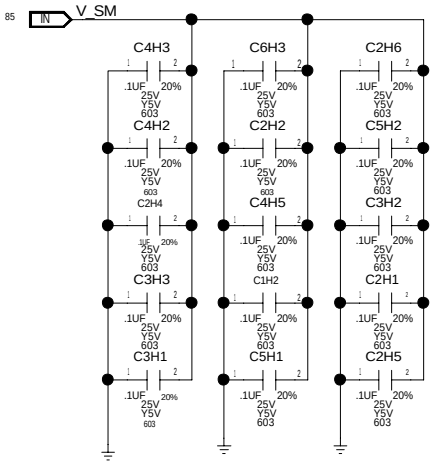




PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND







CHANNEL B

DIMM TO MCH BIT SWAPPING

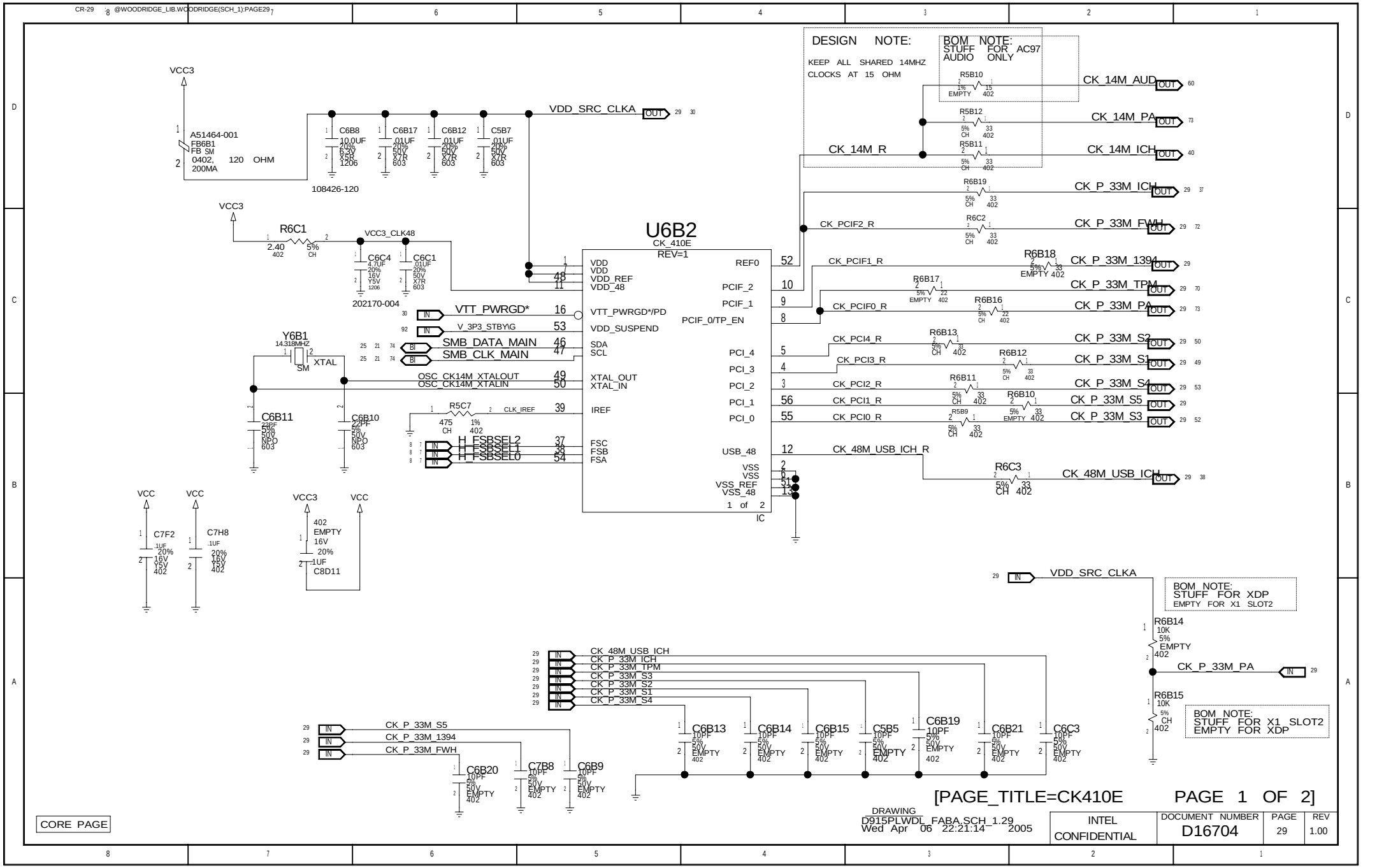
DIMM	MCH	DIMM	MCH
DQ0	DQ5	DQ32	DQ36
DQ1	DQ1	DQ33	DQ33
DQ2	DQ6	DQ34	DQ38
DQ3	DQ3	DQ35	DQ35
DQ4	DQ4	DQ36	DQ37
DQ5	DQ0	DQ37	DQ32
DQ6	DQ7	DQ38	DQ39
DQ7	DQ2	DQ39	DQ34
DQ8	DQ12	DQ40	DQ44
DQ9	DQ13	DQ41	DQ41
DQ10	DQ10	DQ42	DQ46
DQ11	DQ11	DQ43	DQ42
DQ12	DQ8	DQ44	DQ45
DQ13	DQ9	DQ45	DQ40
DQ14	DQ14	DQ46	DQ47
DQ15	DQ15	DQ47	DQ43
DQ16	DQ21	DQ48	DQ52
DQ17	DQ16	DQ49	DQ48
DQ18	DQ23	DQ50	DQ55
DQ19	DQ18	DQ51	DQ51
DQ20	DQ20	DQ52	DQ53
DQ21	DQ17	DQ53	DQ49
DQ22	DQ22	DQ54	DQ54
DQ23	DQ19	DQ55	DQ50
DQ24	DQ28	DQ56	DQ61
DQ25	DQ24	DQ57	DQ57
DQ26	DQ30	DQ58	DQ63
DQ27	DQ26	DQ59	DQ59
DQ28	DQ29	DQ60	DQ60
DQ29	DQ25	DQ61	DQ56
DQ30	DQ31	DQ62	DQ62
DQ31	DQ27	DQ63	DQ58

[PAGE_TITLE=DDR1 DIMM-B 0/1 DCPL]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.28
Wed Apr 06 22:21:14 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	28	1.00


DESIGN NOTE:
KEEP ALL SHARED 14MHZ CLOCKS AT 15 OHM
BOM NOTE: STUFF FOR AC97 AUDIO ONLY
U6B2
CK_410E
REV=1
1 of 2
IC
VCC3
VDD_SRC_CLKA
A51464-001
FB6B1
FB SM
0402, 200MA
120 OHM
108426-120
C6B8 10.0UF 20% 6.3V X5R 1206
C6B17 .01UF 20% 50V X7R 603
C6B12 .01UF 20% 50V X7R 603
C5B7 .01UF 20% 50V X7R 603
R6C1 2.40 5% 402
VCC3_CLK48
C6C4 4.7UF 20% 16V Y5V 1206
C6C1 .01UF 20% 50V X7R 603
202170-004
VTT_PWRGD*
V_3P3_STBY\G
SMB_DATA_MAIN
SMB_CLK_MAIN
Y6B1 14.318MHZ SM XTAL
OSC_CK14M_XTALOUT
OSC_CK14M_XTALIN
C6B11 22PF 5% 50V NPO 603
C6B10 22PF 5% 50V NPO 603
R5C7 475 1% CH 402
CLK_IREF
H_FSBSEL2
H_FSBSEL1
H_FSBSEL0
VDD
VDD_REF
VDD_48
VTT_PWRGD*/PD
VDD_SUSPEND
SDA
SCL
XTAL_OUT
XTAL_IN
IREF
FSC
FSB
FSA
REF0
PCIF_2
PCIF_1
PCIF_0/TP_EN
PCI_4
PCI_3
PCI_2
PCI_1
PCI_0
USB_48
VSS
VSS_REF
VSS_48
CK_14M_R
R5B10 15 1% EMPTY 402
CK_14M_AUD
R5B12 33 5% CH 402
CK_14M_PA
R5B11 33 5% CH 402
CK_14M_ICH
R6B19 33 5% CH 402
CK_P_33M_ICH
CK_PCIF2_R
R6C2 33 5% CH 402
CK_P_33M_FWH
CK_PCIF1_R
R6B18 33 5% EMPTY 402
CK_P_33M_1394
R6B17 22 5% EMPTY 402
CK_P_33M_TPM
CK_PCIF0_R
R6B16 22 5% CH 402
CK_P_33M_PA
CK_PCI4_R
R6B13 33 5% CH 402
CK_P_33M_S2
CK_PCI3_R
R6B12 33 5% CH 402
CK_P_33M_S1
CK_PCI2_R
R6B11 33 5% CH 402
CK_P_33M_S4
CK_PCI1_R
R6B10 33 5% EMPTY 402
CK_P_33M_S5
CK_PCI0_R
R5B9 33 5% CH 402
CK_P_33M_S3
CK_48M_USB_ICH_R
R6C3 33 5% CH 402
CK_48M_USB_ICH
C7F2 .1UF 20% 16V Y5V 402
C7H8 .1UF 20% 16V Y5V 402
C8D11 .1UF 20% 16V 402 EMPTY
VDD_SRC_CLKA
BOM NOTE: STUFF FOR XDP EMPTY FOR X1 SLOT2
R6B14 10K 5% EMPTY 402
CK_P_33M_PA
R6B15 10K 5% CH 402
BOM NOTE: STUFF FOR X1 SLOT2 EMPTY FOR XDP
CK_48M_USB_ICH
CK_P_33M_ICH
CK_P_33M_TPM
CK_P_33M_S3
CK_P_33M_S2
CK_P_33M_S1
CK_P_33M_S4
CK_P_33M_S5
CK_P_33M_1394
CK_P_33M_FWH
C6B13 10PF 5% 50V EMPTY 402
C6B14 10PF 5% 50V EMPTY 402
C6B15 10PF 5% 50V EMPTY 402
C5B5 10PF 5% 50V EMPTY 402
C6B19 10PF 5% 50V EMPTY 402
C6B21 10PF 5% 50V EMPTY 402
C6C3 10PF 5% 50V EMPTY 402
C6B20 10PF 5% 50V EMPTY 402
C7B8 10PF 5% 50V EMPTY 402
C6B9 10PF 5% 50V EMPTY 402
[PAGE_TITLE=CK410E PAGE 1 OF 2]
CORE PAGE
DRAWING
D915PLWDL_FABA.SCH_1.29
Wed Apr 06 22:21:14 2005
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 29
REV 1.00

DESIGN NOTE:
STUFF FOR EVALUATION OF COST REDUCTION ON VOLTAGE SOURCE

CAD NOTE:
PLACE (1) PER PIN

DESIGN NOTE:
SATA MUST BE ON PIN_26, PIN_27

DESIGN NOTE:
REMOVE OFF-PAGE FOR UATX

CORE PAGE

VREG FEATURE

LOCATION	X1 SLOT2	XDP
R5C12	STUFF	EMPTY
R5C13	STUFF	EMPTY
R5C15	EMPTY	STUFF
R5C16	EMPTY	STUFF

DRAWING
D915PLWDL_FABA.SCH_1.30
Wed Apr 06 22:21:14 2005

[PAGE_TITLE=CK410E PAGE 2 OF 2]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	30	1.00

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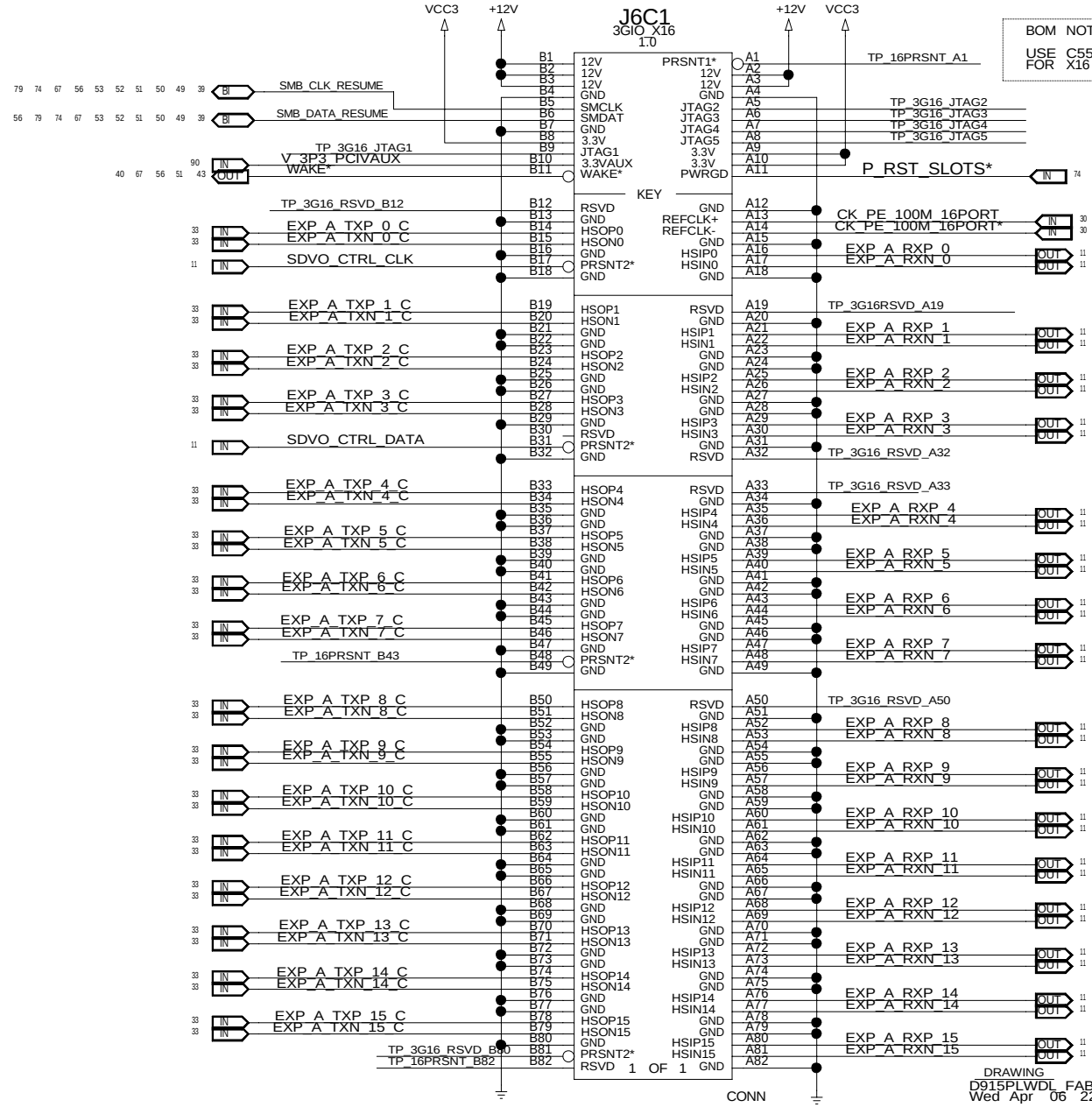
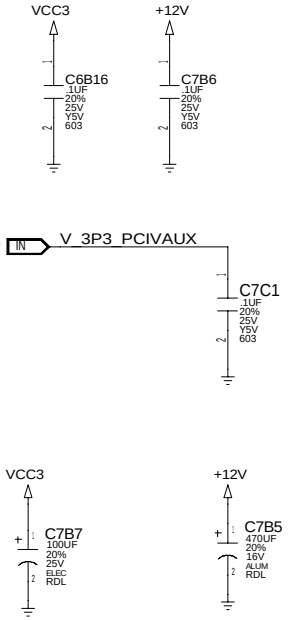
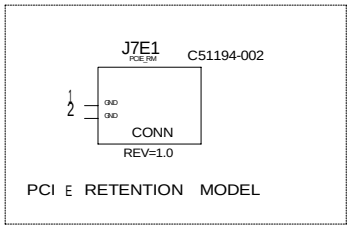
PCI EXPRESS
16-PORT

BOM NOTE:
USE C55845-002
FOR X16 CONN

J6C1
3GIO_X16
1.0







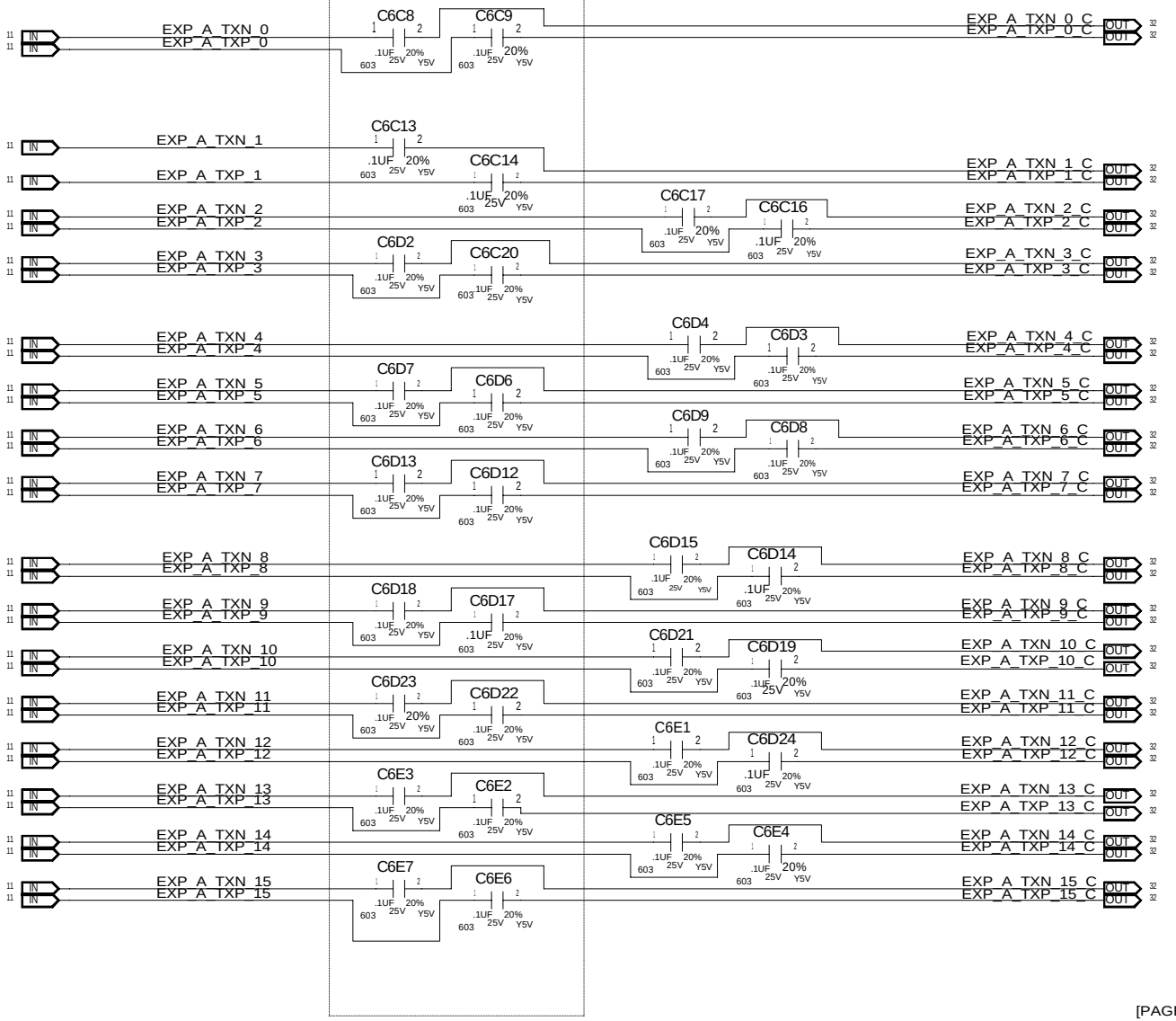
CORE PAGE

[PAGE_TITLE=PCIE 16-PORT]

DRAWING
D915PLWDL_FABA.SCH_1.32
Wed Apr 06 22:21:14 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	32	1.00

BOM NOTE:
ALWAYS STUFF



[PAGE_TITLE=PCIE COUPLING]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.33
Wed Apr 06 22:21:15 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	33	1.00

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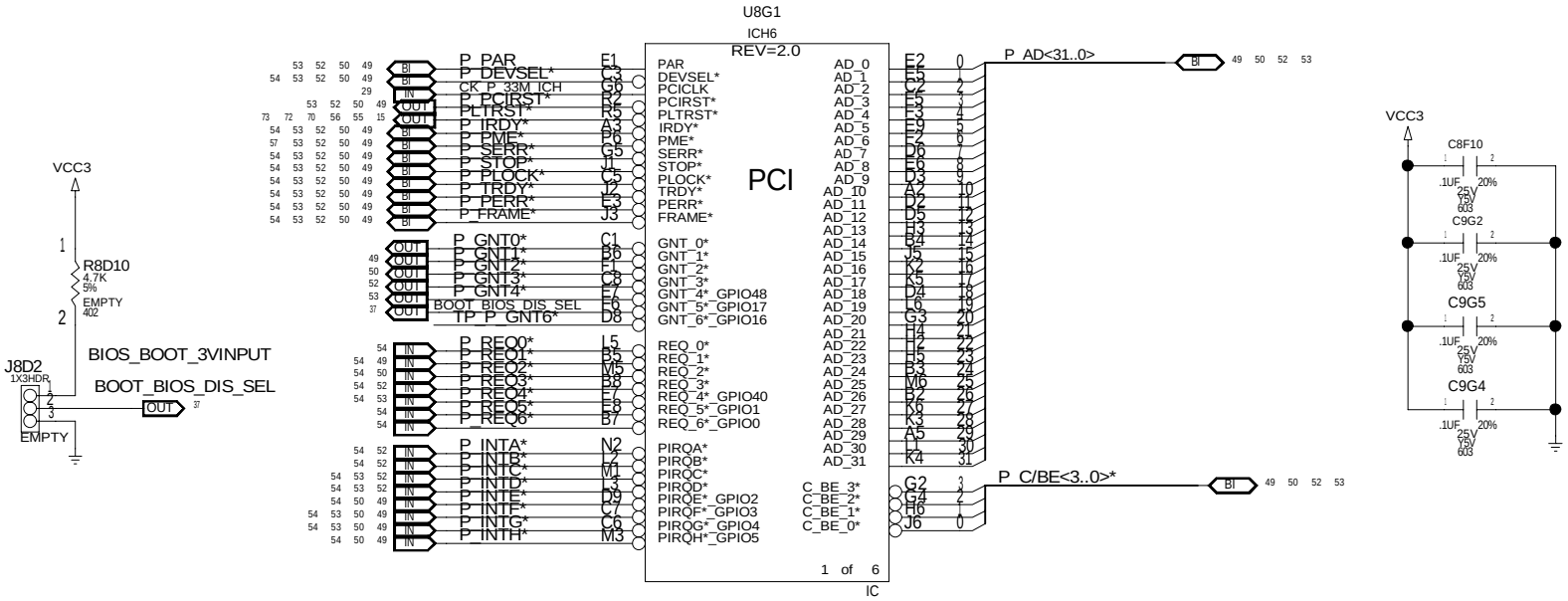


CAD NOTE:

PLACE 1 EACH NEAR A3 & F1.
PLACE REMAINDER ANYWHERE

[PAGE_TITLE=ICH 1 OF 6 - CONTROL]

DRAWING
D915PLWDL_FABA.SCH_1.37
Wed Apr 06 22:21:15 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	37	1.00

DESIGN NOTE:
FOR PCI_E X1 SLOT 1

38 IN HSO_P0 1 C7G5 2 HSO_P0_C OUT 51
.1UF 20% 25V Y5V 603

38 IN HSO_N0 1 C7G3 2 HSO_N0_C OUT 51
.1UF 20% 25V Y5V 603

U8G1
ICH6
REV=2.0

11	IN	DMI_MTN_IRN_0	T25	DMI_0RXN	USBP_0N	C21	USB_FRONT1*
11	IN	DMI_MTP_IRP_0	T24	DMI_0RXP	USBP_0P	D21	USB_FRONT1
11	OUT	DMI_ITN_MRN_0	R27	DMI_0TXN	USBP_1N	A20	USB_FRONT2*
11	OUT	DMI_ITP_MRP_0	R26	DMI_0TXP	USBP_1P	B20	USB_FRONT2
11	IN	DMI_MTN_IRN_1	V25	DMI_1RXN	USBP_2N	D19	USB_BACK4*
11	IN	DMI_MTP_IRP_1	V24	DMI_1RXP	USBP_2P	C19	USB_BACK4
11	OUT	DMI_ITN_MRN_1	U27	DMI_1TXN	USBP_3N	A18	USB_FRONT3*
11	OUT	DMI_ITP_MRP_1	U26	DMI_1TXP	USBP_3P	B18	USB_FRONT3
11	IN	DMI_MTN_IRN_2	Y25	DMI_2RXN	USBP_4N	E17	USB_BACK3*
11	IN	DMI_MTP_IRP_2	Y24	DMI_2RXP	USBP_4P	D17	USB_BACK3
11	OUT	DMI_ITN_MRN_2	W27	DMI_2TXN	USBP_5N	B16	USB_FRONT4*
11	OUT	DMI_ITP_MRP_2	W26	DMI_2TXP	USBP_5P	A16	USB_FRONT4
11	IN	DMI_MTN_IRN_3	AB24	DMI_3RXN	USBP_6N	C15	USB_BACK2*
11	IN	DMI_MTP_IRP_3	AB23	DMI_3RXP	USBP_6P	D15	USB_BACK2
11	OUT	DMI_ITN_MRN_3	AA27	DMI_3TXN	USBP_7N	A14	USB_BACK1*
11	OUT	DMI_ITP_MRP_3	AA26	DMI_3TXP	USBP_7P	B14	USB_BACK1

51	IN	HSI_N0	H25	PERN_1	OC_0*	C27	USB_OC_FRONT12*
51	IN	HSI_P0	H24	PERP_1	OC_1*	B27	
38	OUT	HSO_N0	G27	PETN_1	OC_2*	B26	USB_OC_FRONT34_BACK56*
38	OUT	HSO_P0	G26	PETP_1	OC_3*	C23	USB_OC_BACK_RIGHT*
	IN	HSI_N1	K25	PERN_2	OC_4*_GPIO9	D23	
	IN	HSI_P1	K24	PERP_2	OC_5*_GPIO10	C25	
	OUT	HSO_N1	J27	PETN_2	OC_6*_GPIO14	C24	USB_OC_BACK_LEFT*
	OUT	HSO_P1	J26	PETP_2	OC_7*_GPIO15		
67	IN	HSI_N2	M25	PERN_3		B22	
67	IN	HSI_P2	M24	PERP_3	USBRBIAS	A22	USBRBIAS_ICH
38	OUT	HSO_N2	L27	PETN_3	USBRBIAS*		
38	OUT	HSO_P2	L26	PETP_3	CLK48	A27	
		TP_HSI_N3	P24	PERN_4			
		TP_HSI_P3	P23	PERP_4			
38	OUT	HSO_N3	N27	PETN_4			
38	OUT	HSO_P3	N26	PETP_4			

DMI
PCI EXPRESS
USB

			E24	DMI_ZCOMP			
			E23	DMI_IRCOMP			
			AD25	DMI_CLKN			
			AC25	DMI_CLKP			

2 of 6

41 IN V_PCIEXPRESS_PWR 1 R7G1 2 DMICOMP_ICH
402 24.9 CH 1%

CAD NOTE:
CONNECT TRACES TOGETHER CLOSE TO ICH PINS

30 IN CK_PE_100M_ICH*
30 IN CK_PE_100M_ICH

USBRBIAS_ICH 1 R8F12 2
402 22.6 CH 1%

CAD NOTE:
TRACES TIED TOGETHER CLOSE TO PINS
LENGTH NO LONGER THAN 200 MIL TO RESISTOR

CK_48M_USB_ICH IN 29

DESIGN NOTE: FOR PCI_E X1 SLOT 2 (ATX)

38 IN HSO_P2 1 C7G9 2 HSO_P2_C OUT 67
.1UF 20% 25V Y5V 603

38 IN HSO_N2 1 C7G6 2 HSO_N2_C OUT 67
.1UF 20% 25V Y5V 603

38 IN HSO_P3 1 C7G11 2 TP_HSO_P3_C
.1UF 20% 25V 603 EMPTY

38 IN HSO_N3 1 C7G10 2 TP_HSO_N3_C
.1UF 20% 25V 603 EMPTY

USB CLASSIC FILTER

92 IN V_3P3_STBY\G
C8F12 .1UF 10% 16V X7R 603
C8F13 .1UF 10% 16V X7R 603

CAD NOTE:
PLACE (2) 0.1UF NEAR A17
PLACE 0.01UF NEAR A24

USB HS (HI-SPEED) FILTER

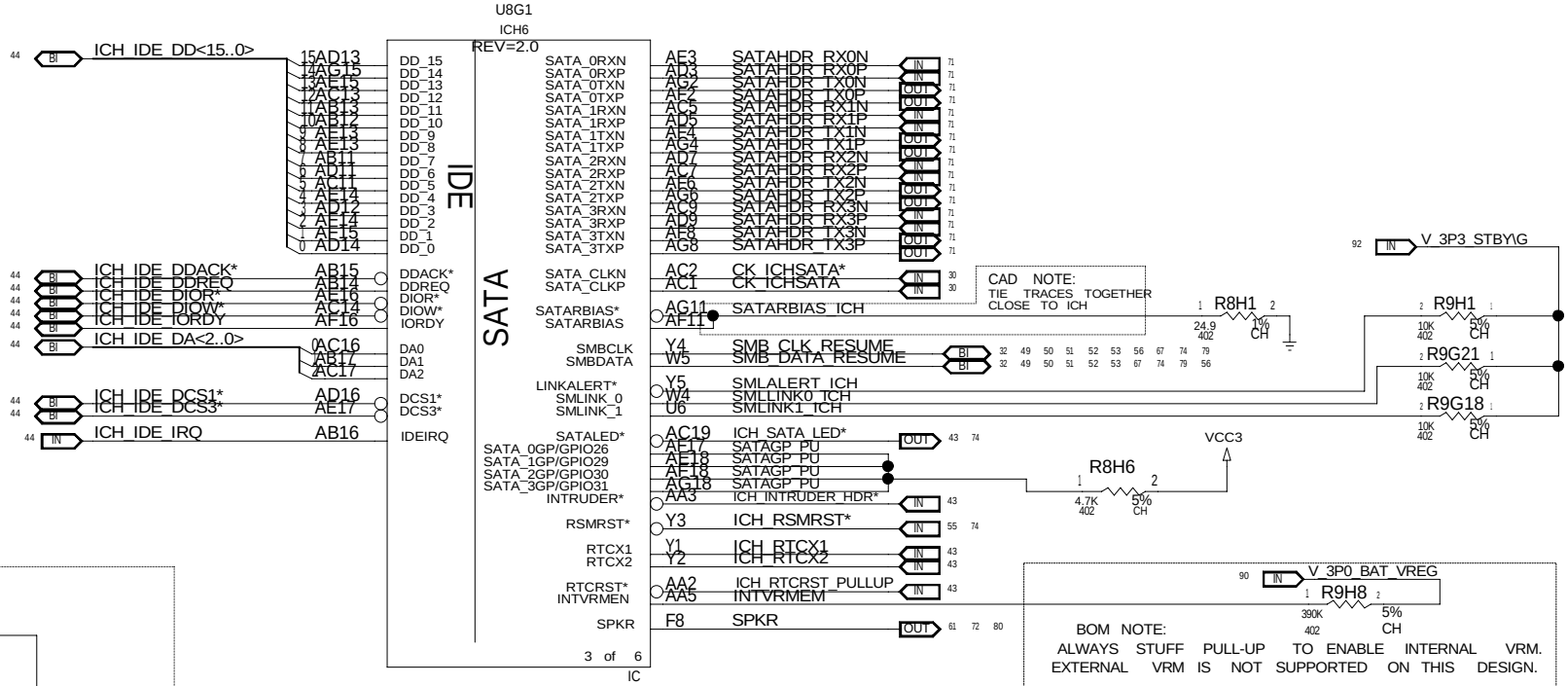
102 IN V_1P5_CORE
C7F12 .01UF 20% 50V X7R 603
C7F11 .1UF 10% 16V X7R 603

CAD NOTE:
PLACE 0.01UF NEAR A25
PLACE 0.1UF NEAR D27

DRAWING
D915PLWDL_FABA.SCH_1.38
Wed Apr 06 22:21:15 2005

[PAGE_TITLE=ICH 2 OF 6 - CONTROL]

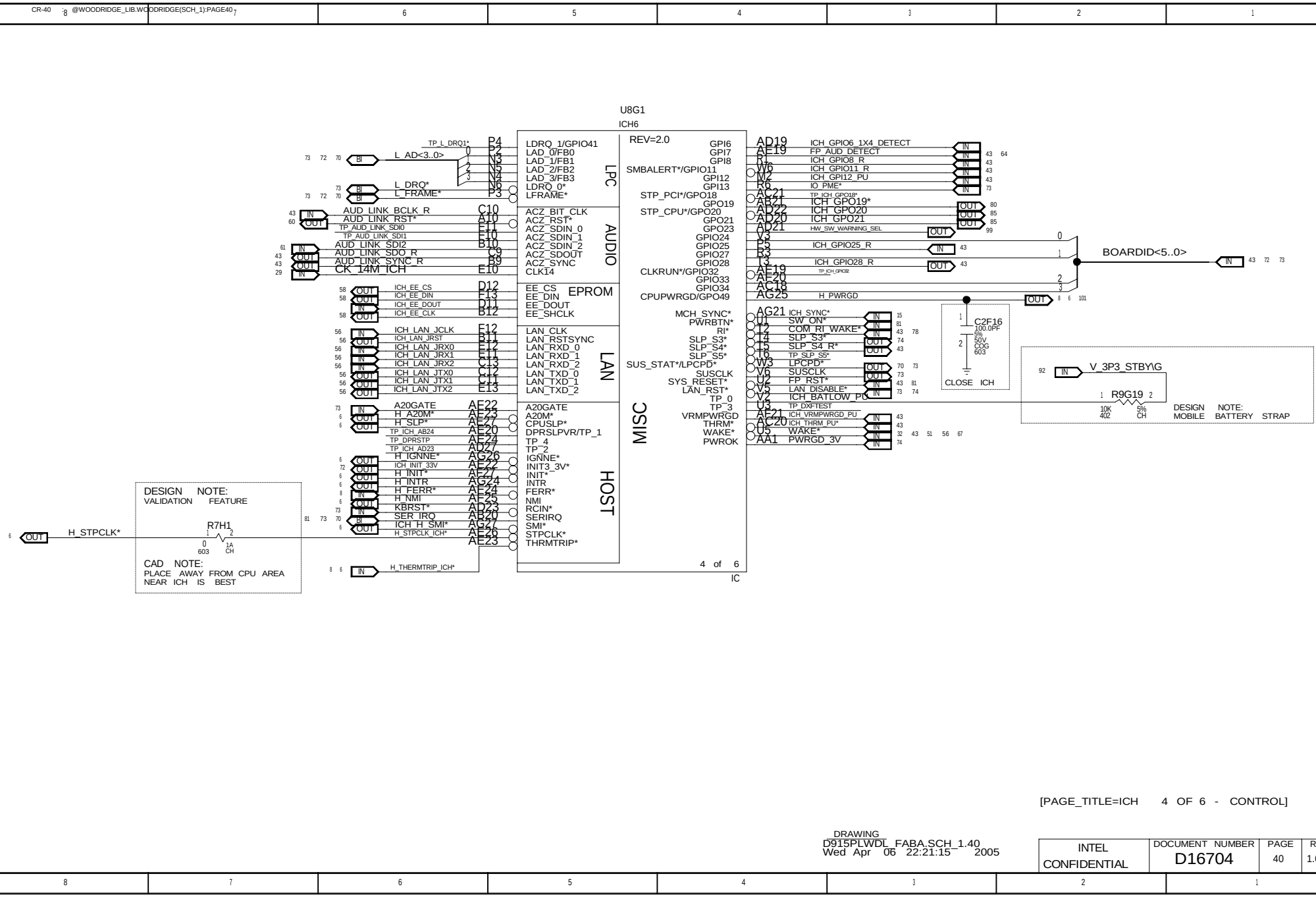
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	38	1.00



[PAGE_TITLE=ICH 3 OF 6 - CONTROL]

DRAWING
D915PLWDL_FABA.SCH_1.39
Wed Apr 06 22:21:15 2005

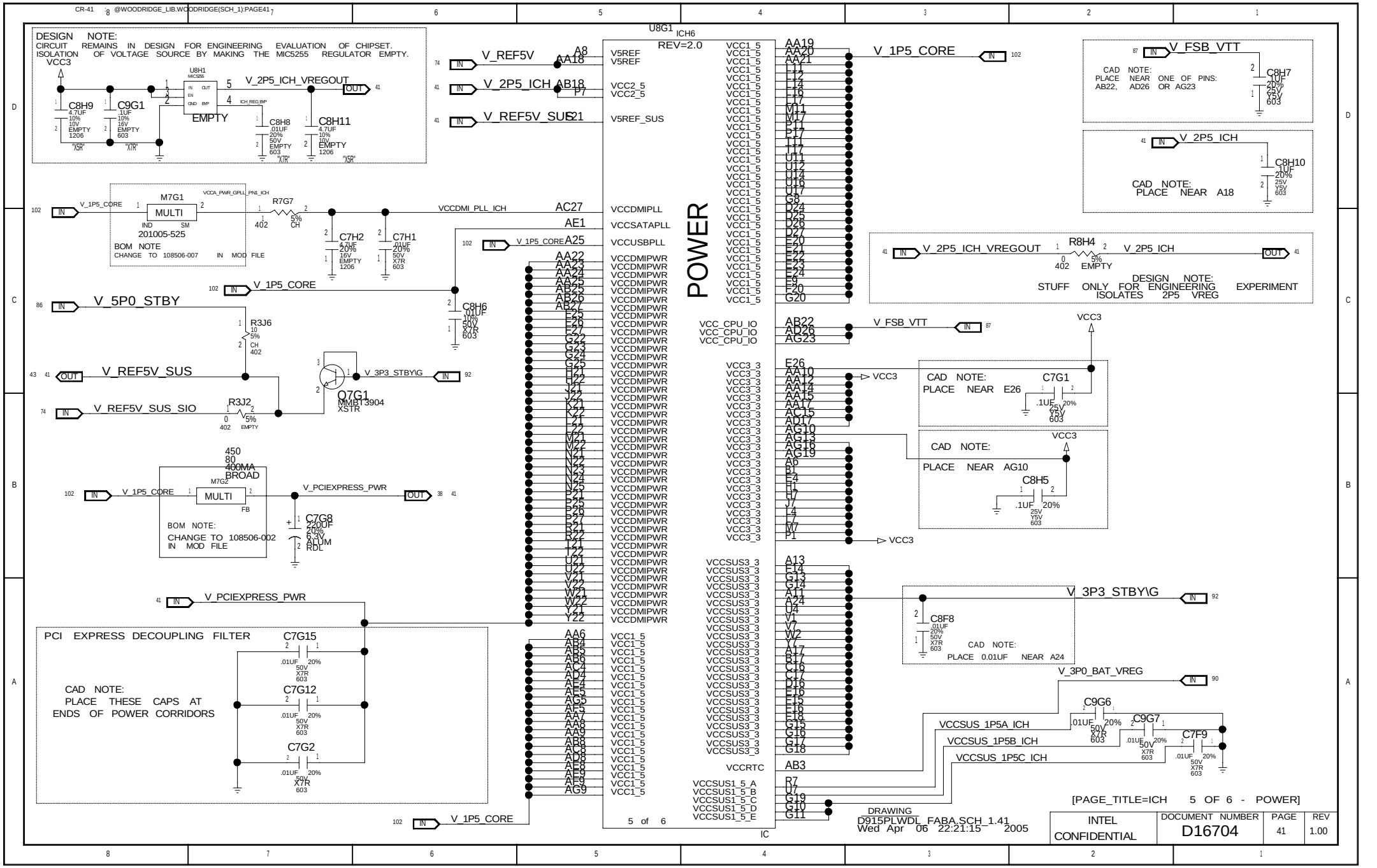
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	39	1.00

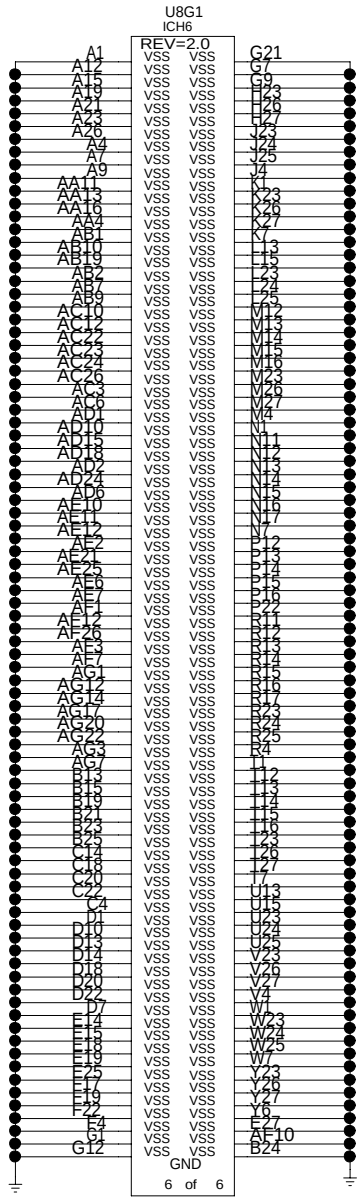


[PAGE_TITLE=ICH 4 OF 6 - CONTROL]

DRAWING
D915PLWDL_FABA.SCH_1.40
Wed Apr 06 22:21:15 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	40	1.00


DESIGN NOTE:
CIRCUIT REMAINS IN DESIGN FOR ENGINEERING EVALUATION OF CHIPSET.
ISOLATION OF VOLTAGE SOURCE BY MAKING THE MIC5255 REGULATOR EMPTY.
U8G1
ICH6
REV=2.0
POWER
V_REF5V
V_2P5_ICH
V_REF5V_SUS
V_1P5_CORE
V_FSB_VTT
V_2P5_ICH_VREGOUT
V_5P0_STBY
V_REF5V_SUS_SIO
V_3P3_STBY\G
V_PCIEXPRESS_PWR
V_3P0_BAT_VREG
VCCDMI_PLL_ICH
VCCSUS_1P5A_ICH
VCCSUS_1P5B_ICH
VCCSUS_1P5C_ICH
VCC3
PCI EXPRESS DECOUPLING FILTER
CAD NOTE:
PLACE THESE CAPS AT
ENDS OF POWER CORRIDORS
BOM NOTE
CHANGE TO 108506-007 IN MOD FILE
201005-525
DESIGN NOTE:
STUFF ONLY FOR ENGINEERING EXPERIMENT
ISOLATES 2P5 VREG
CAD NOTE:
PLACE NEAR A18
PLACE NEAR AB22, AD26 OR AG23
PLACE NEAR E26
PLACE NEAR AG10
PLACE 0.01UF NEAR A24
BOM NOTE:
CHANGE TO 108506-002
IN MOD FILE
DRAWING
D915PLWDL_FABA.SCH_1.41
Wed Apr 06 22:21:15 2005
[PAGE_TITLE=ICH 5 OF 6 - POWER]
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 41
REV 1.00



HS8G1
C46655-001
ICH6_HSK
NC_1
NC_2
NC_3
NC_4
EMPTY

NOTE:
NO PHYSICAL PINS
ON ALLEGRO MODEL

TH
J9H1
NC
EMPTY
A13494-005

TH
J7F1
NC
EMPTY
A13494-005

DRAWING
D915PLWDL_FABA.SCH_1.42
Wed Apr 06 22:21:16 2005

[PAGE_TITLE=ICH 6 OF 6 - GROUND]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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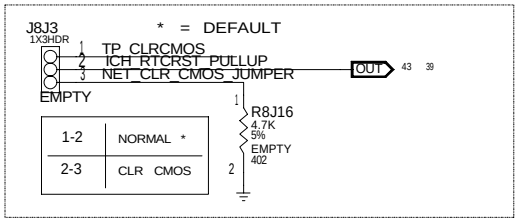
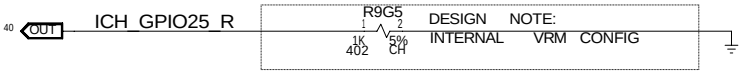
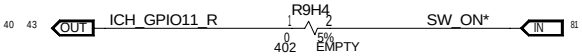
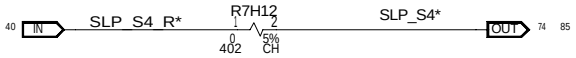
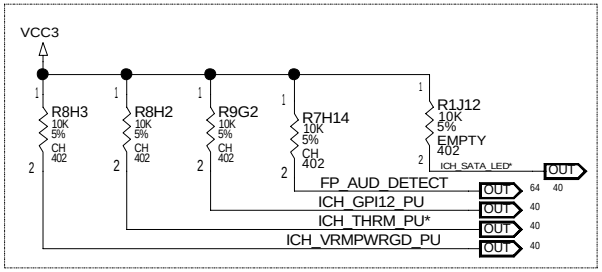
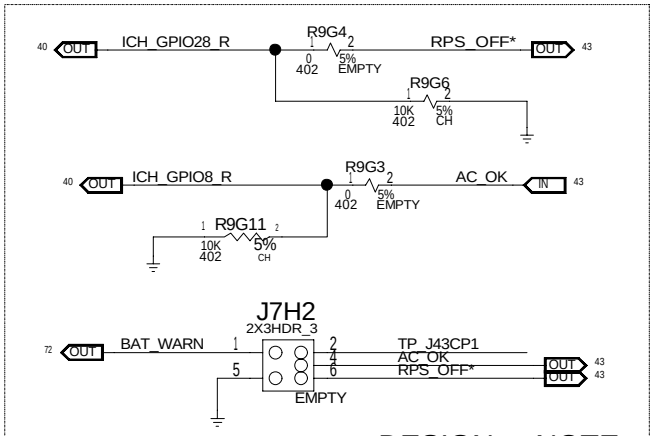


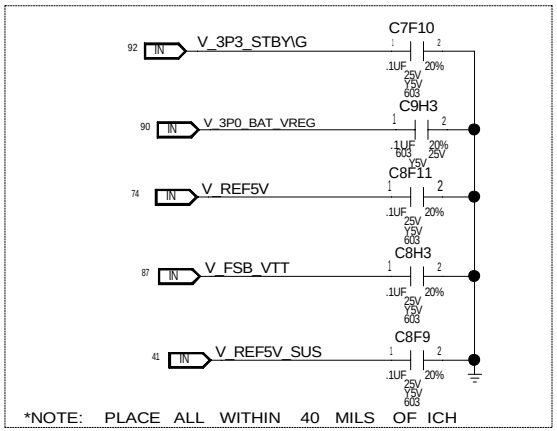


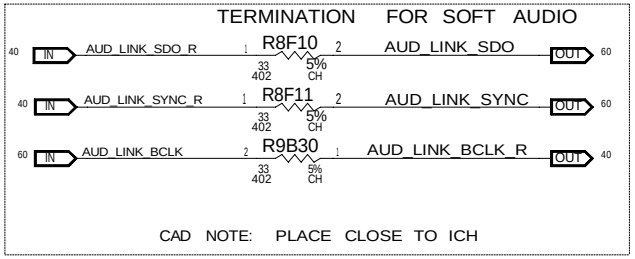


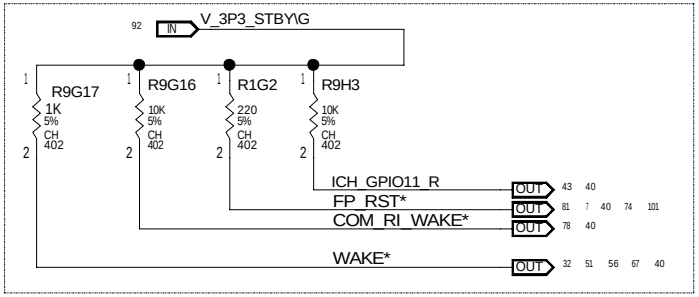


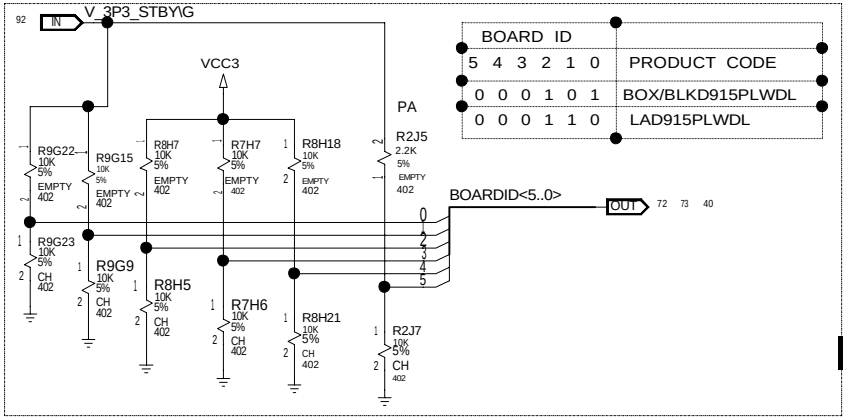




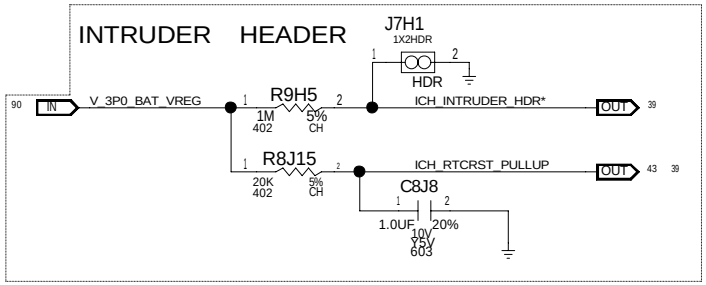




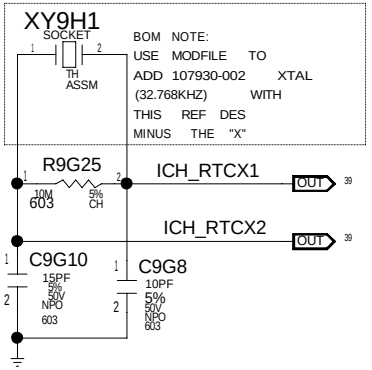




BOARD ID	
5 4 3 2 1 0	PRODUCT CODE
0 0 0 1 0 1	BOX/BLKD915PLWDL
0 0 0 1 1 0	LAD915PLWDL



FLIP-LID XTAL HOLDER USES STANDARD XTAL.



ICH PULLUPS & DECOUPLING

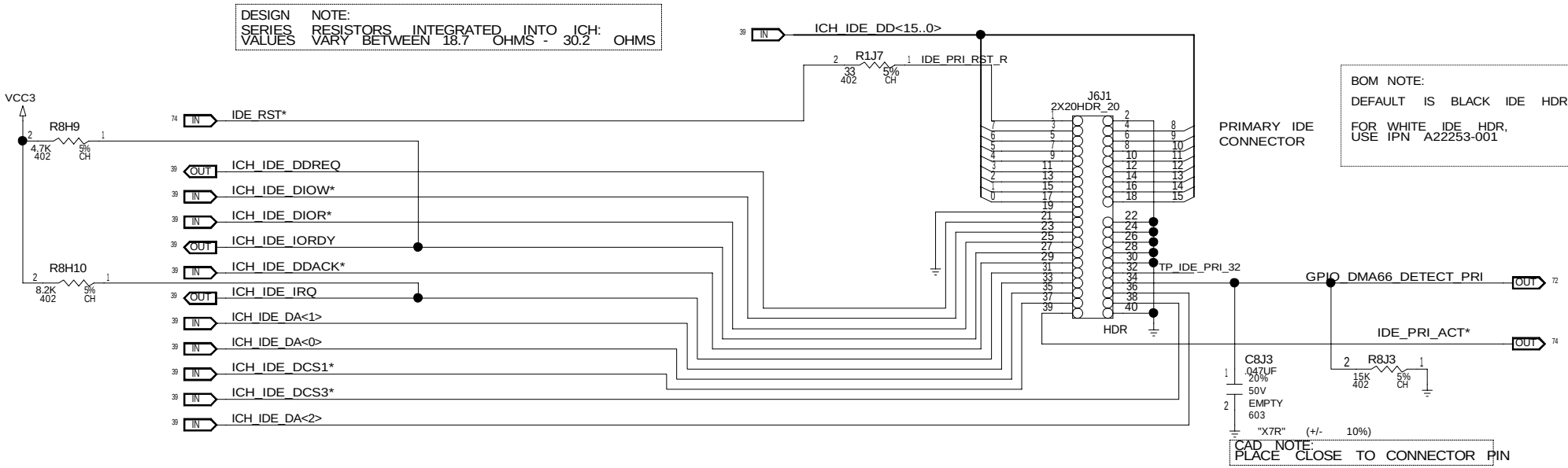
[PAGE_TITLE=ICH TERMINATION]

DRAWING
D915PLWDL_FABA.SCH_1.43
Thu Apr 07 13:40:20 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	43	1.00

DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

BOM NOTE:
DEFAULT IS BLACK IDE HDR.
FOR WHITE IDE HDR, USE IPN A22253-001



CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

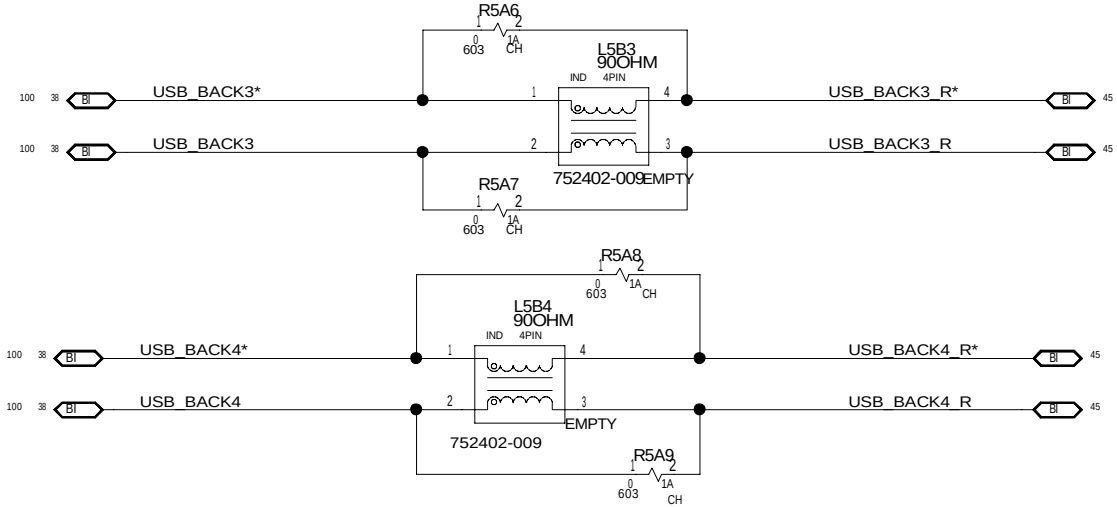
[PAGE_TITLE=IDE_SOUTH_BRIDGE]

DRAWING
D915PLWDL_FABA.SCH_1.44
Wed Apr 06 22:21:16 2005

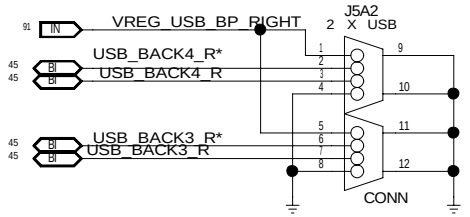
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	44	1.00

PCI IDE

CAD NOTE:
OVERLAPPING FOOTPRINTS
DO NOT CHANGE TO 402



DOUBLE STACK USB

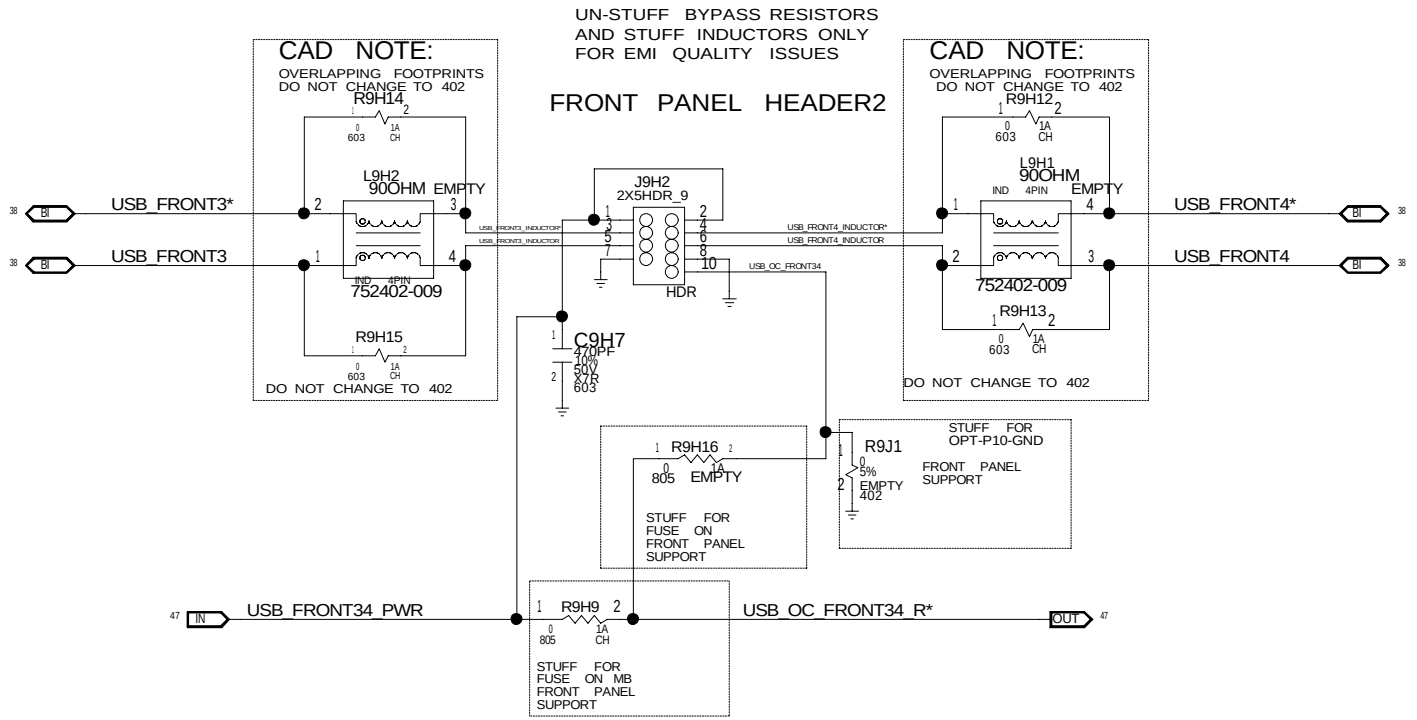


[PAGE_TITLE=USB_BACKPANEL_CONN]

DRAWING
D915PLWDL_FABA.SCH_1.45
Thu Apr 07 17:12:06 2005

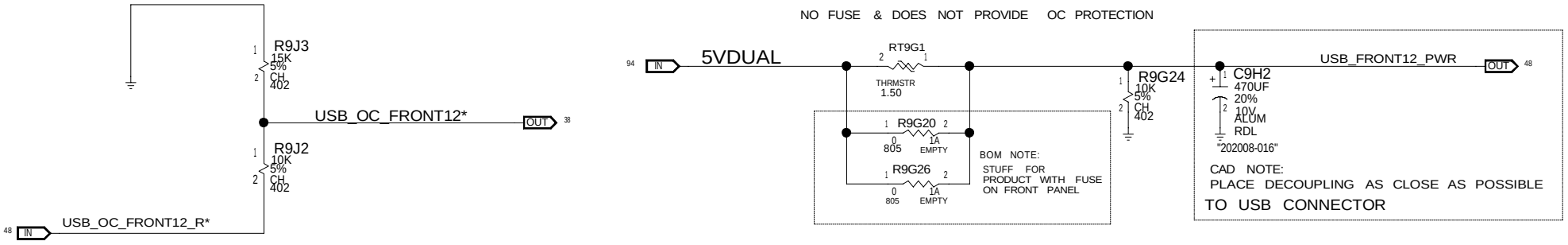
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	45	1.00

USB FRONT PANEL HEADER #2

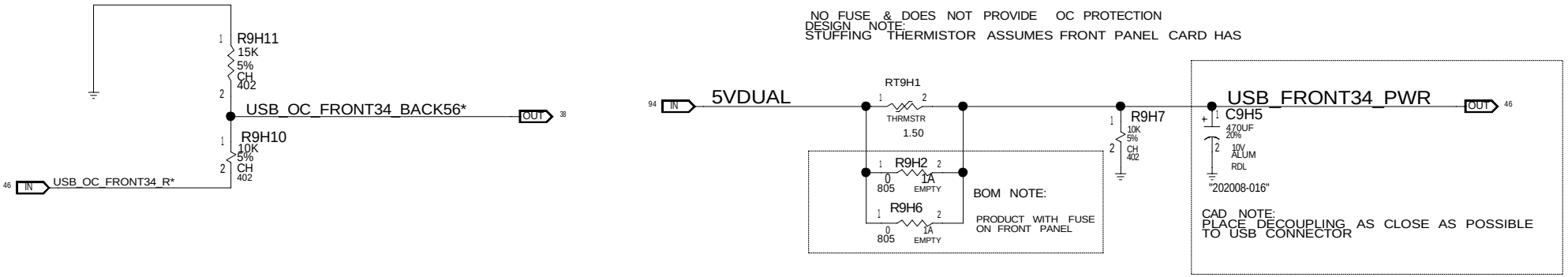


[PAGE_TITLE=USB_FP #2 HEADER]

POWER FOR USB FRONT PANEL #1



POWER FOR USB FRONT PANEL #2



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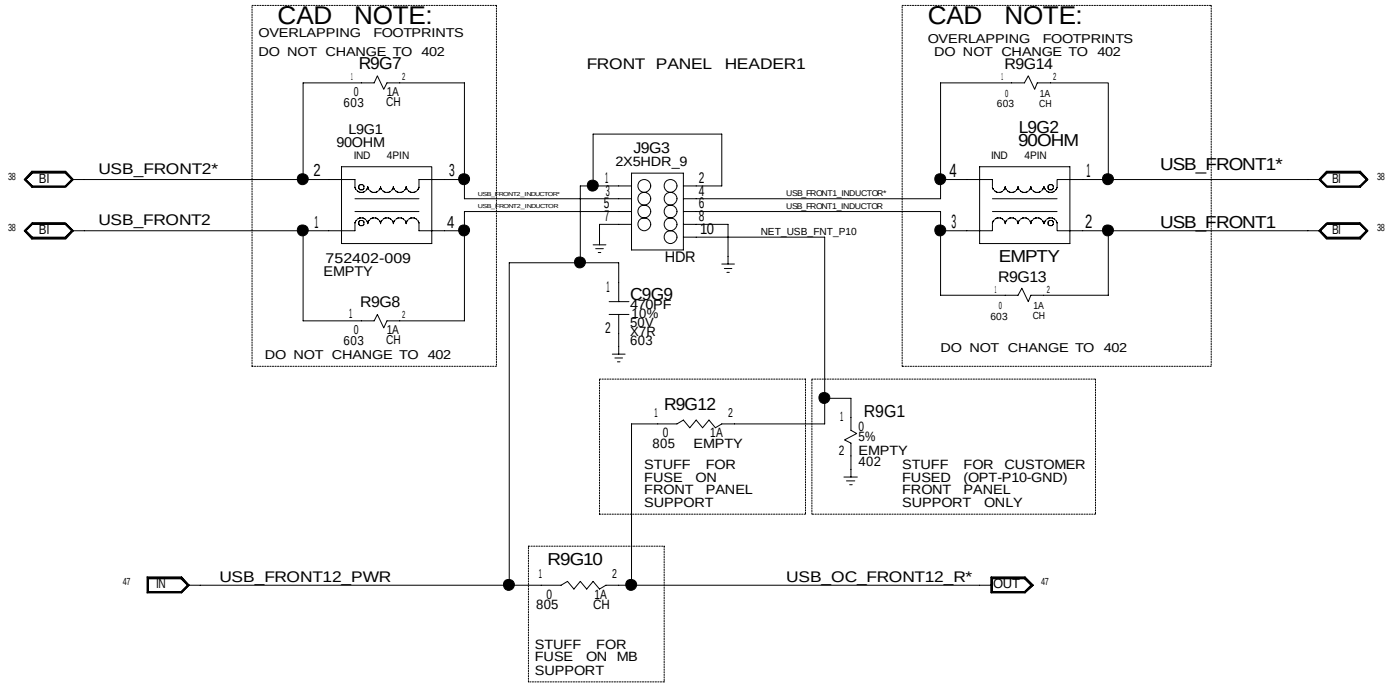
DRAWING
D915PLWDL_FABA.SCH 1.47
Wed Apr 06 22:21:16 2005

USB FRONT PANEL HEADER #1



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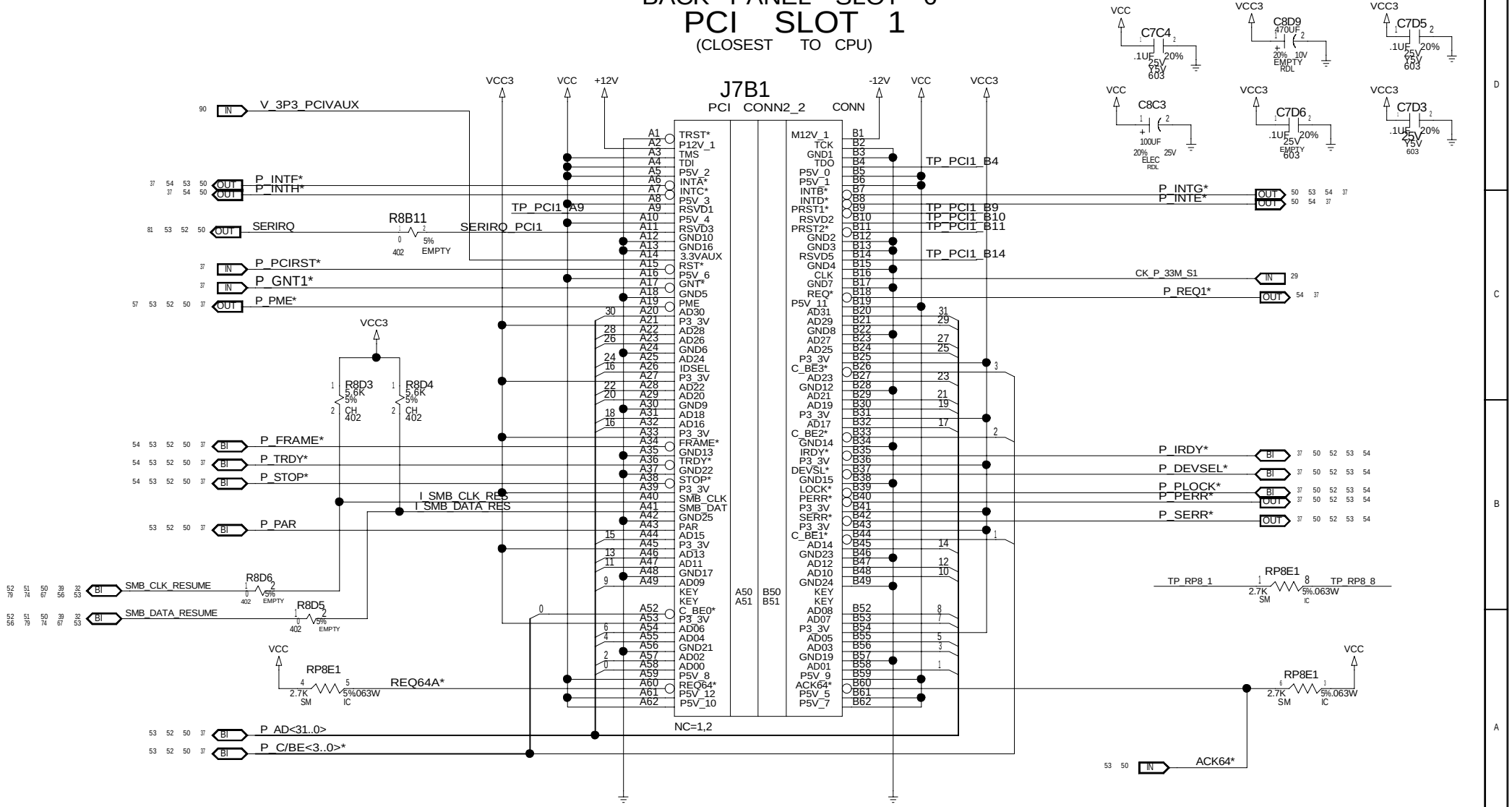
DRAWING
D915PLWDL_FABA.SCH_1.48
Wed Apr 06 22:21:16 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	48	1.00

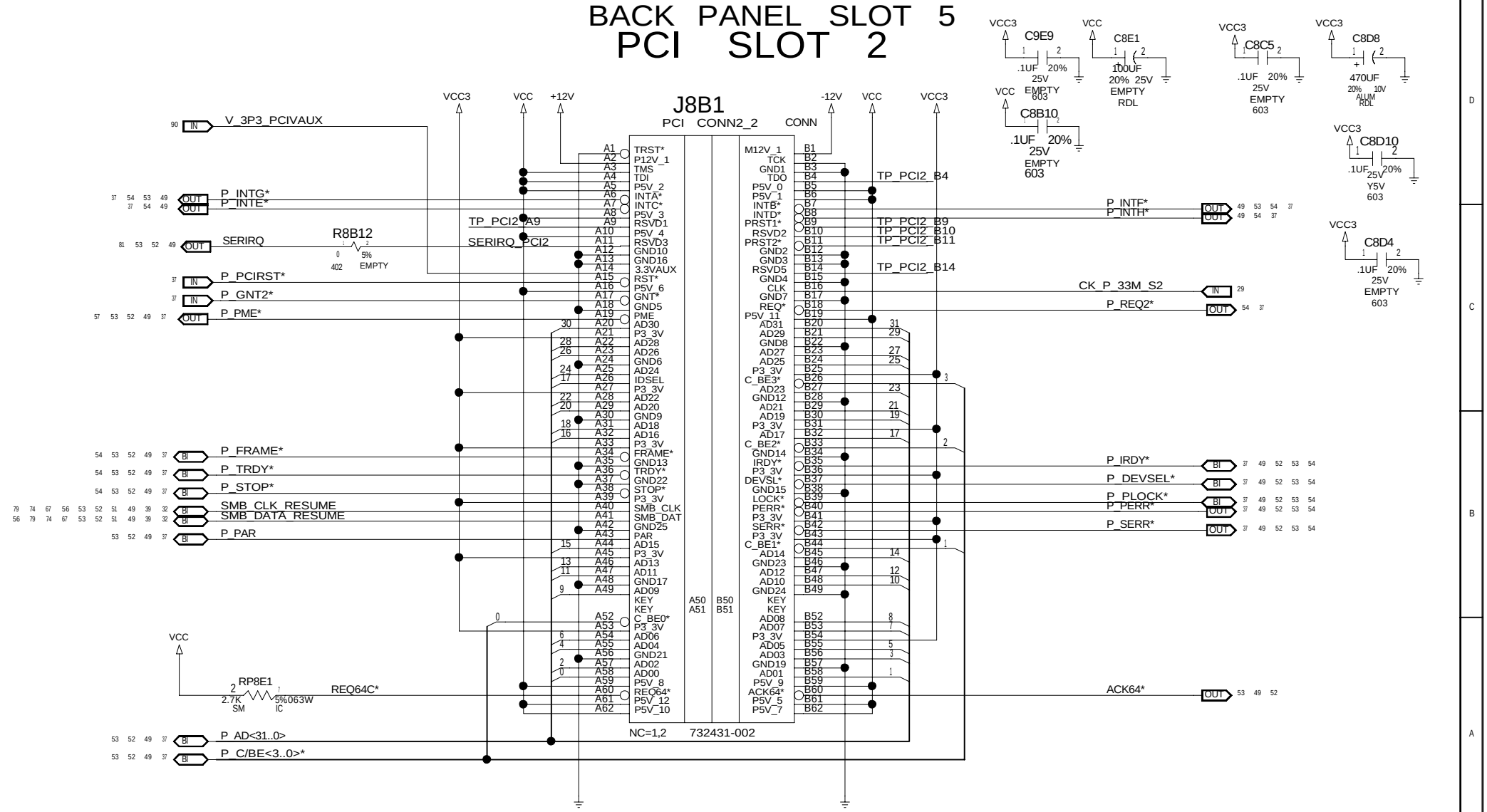
BACK PANEL SLOT 6
PCI SLOT 1
(CLOSEST TO CPU)



[PAGE_TITLE=PCI_CONN_1]

DRAWING				
D915PLWDL_FABA.SCH_1.49 Wed Apr 06 22:21:17 2005	INTEL CONFIDENTIAL	DOCUMENT NUMBER D16704	PAGE 49	REV 1.00

BACK PANEL SLOT 5
PCI SLOT 2



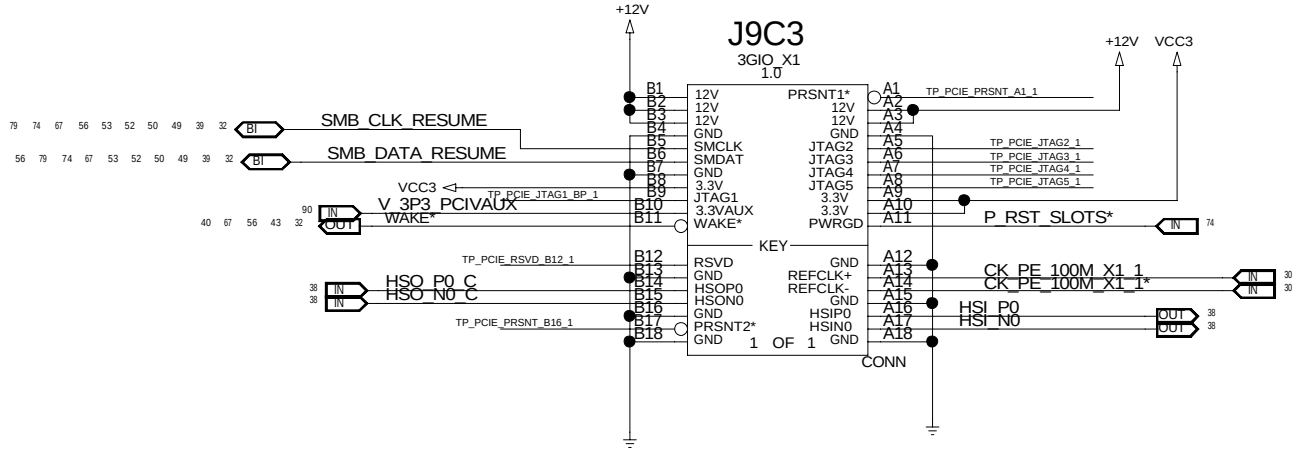
[PAGE_TITLE=PCI_CONN_2]

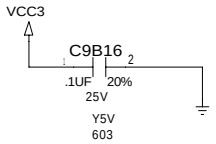
DRAWING
D915PLWDL_FABA.SCH_1.50
Wed Apr 06 22:21:17 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	50	1.00

BACK PANEL SLOT 4
PCI EXPRESS X1 SLOT 1

BOM NOTE:
USE C55845-001
FOR X1 CONN





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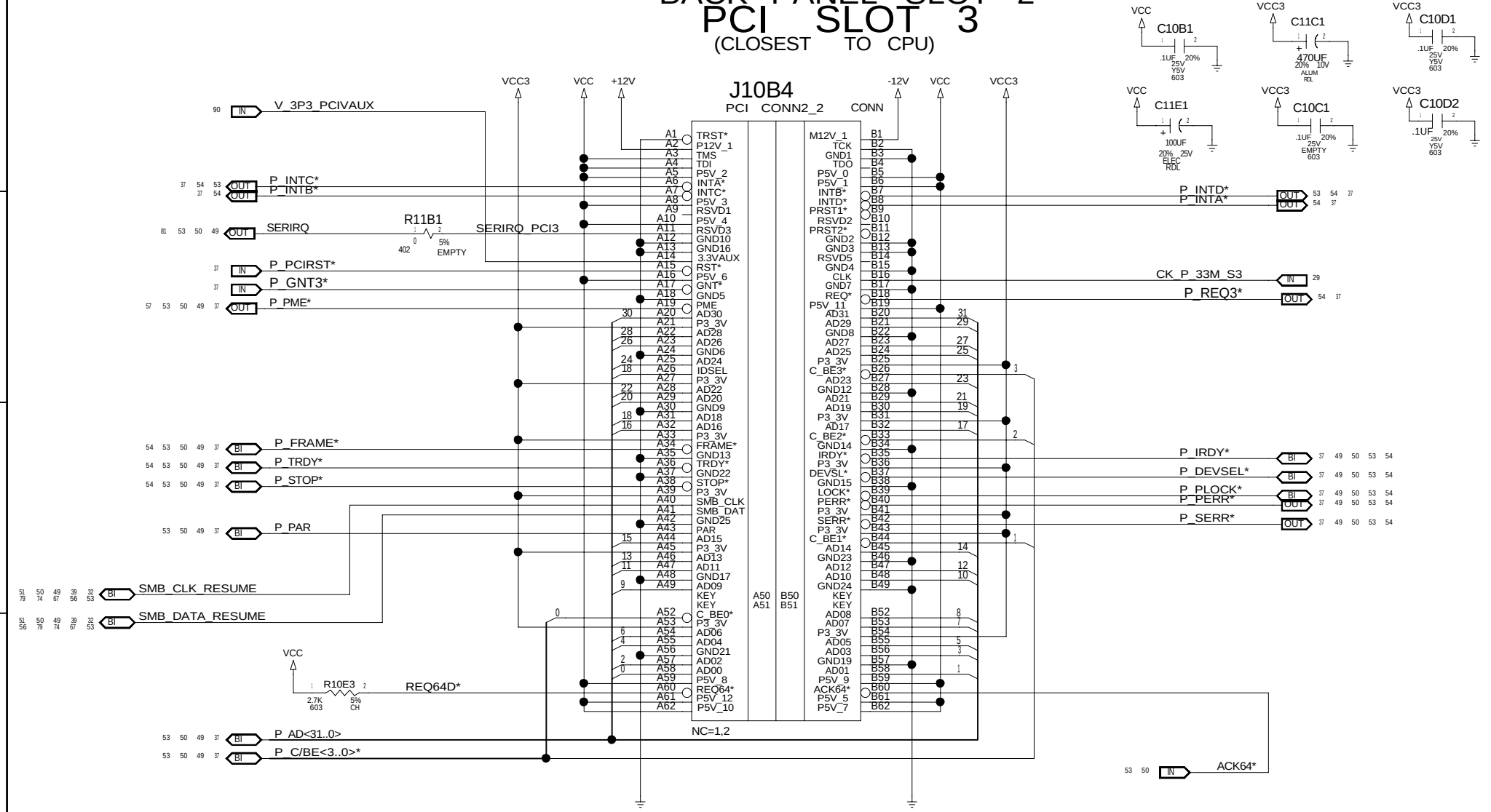
DRAWING
D915PLWDL_FABA.SCH_1.51
Wed Apr 06 22:21:17 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	51	1.00

BACK PANEL SLOT 2
PCI SLOT 3
(CLOSEST TO CPU)



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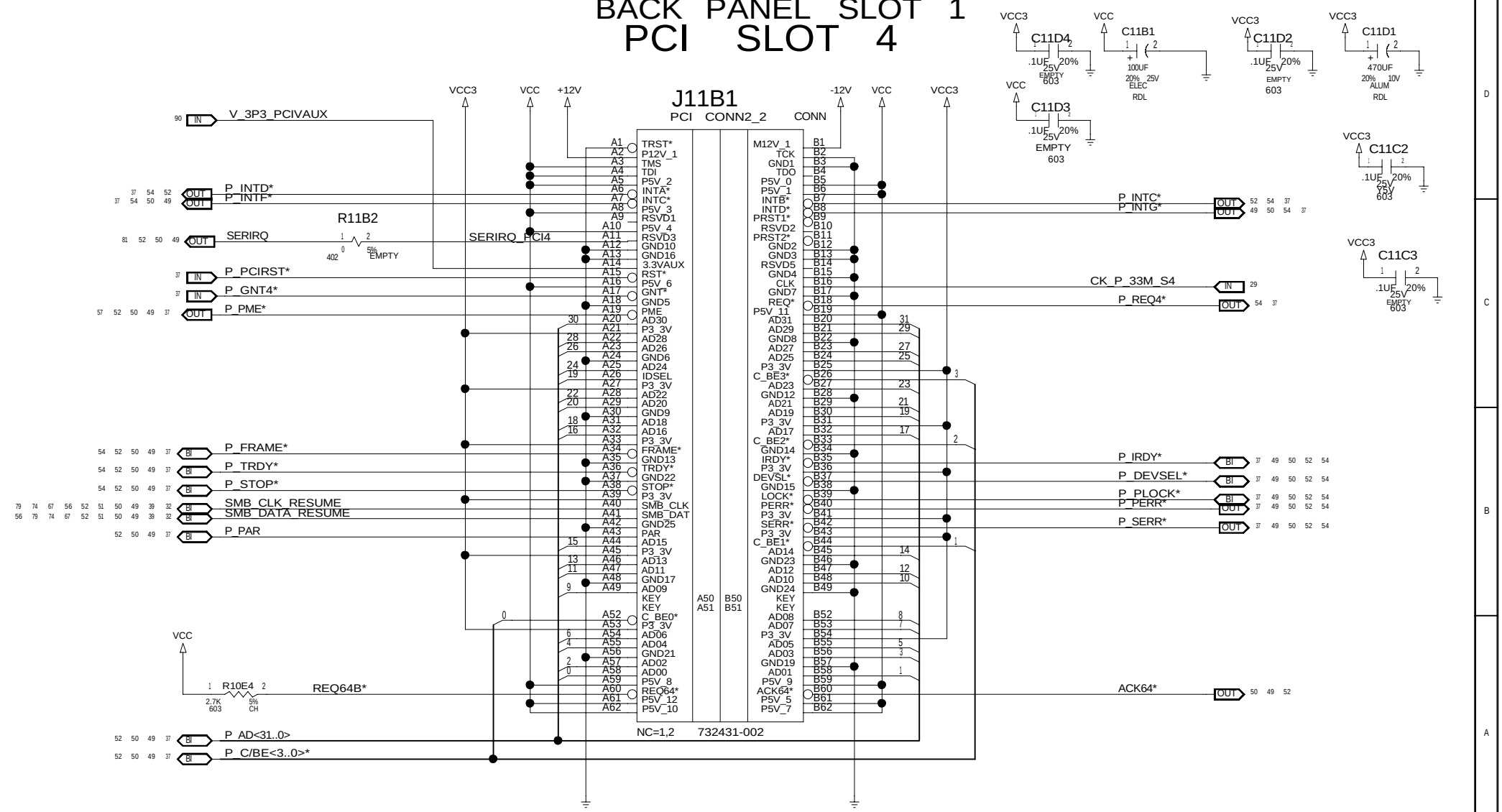
D915PLWDL_FABA.SCH_1.52
Thu Apr 07 19:35:30 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	52	1.00

BACK PANEL SLOT 1
PCI SLOT 4



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DRAWING
D915PLWDL_FABA.SCH_1.53
Thu Apr 07 17:11:05 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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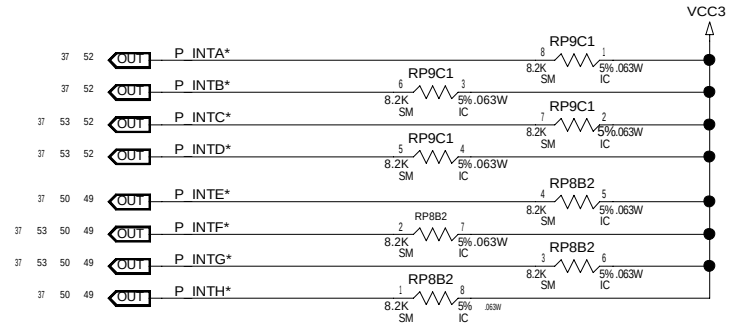

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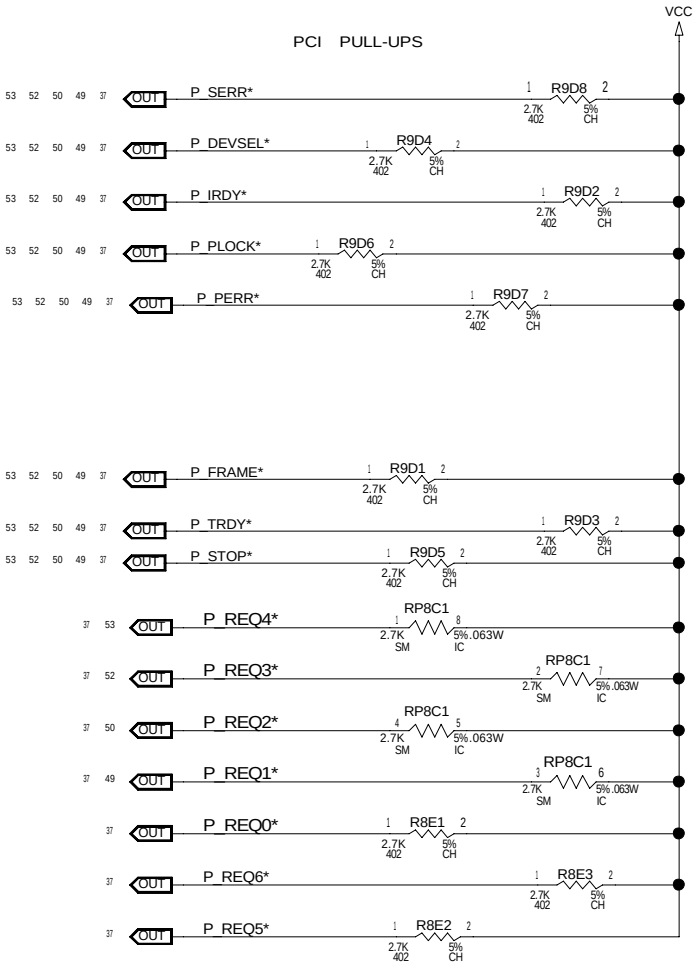

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Wed Apr 06 22:21:18 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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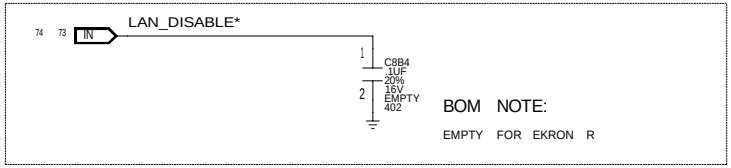
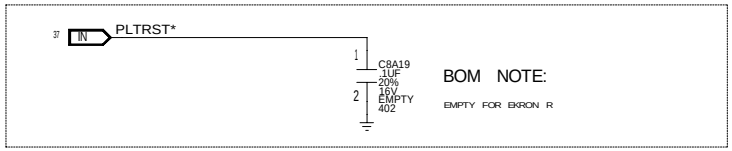
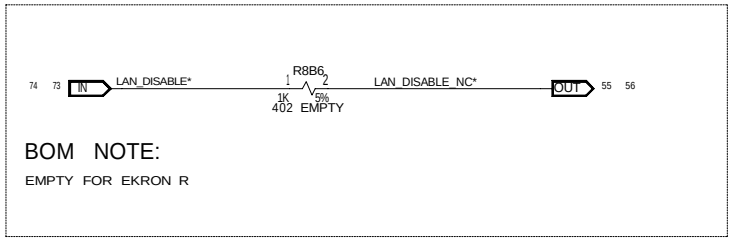
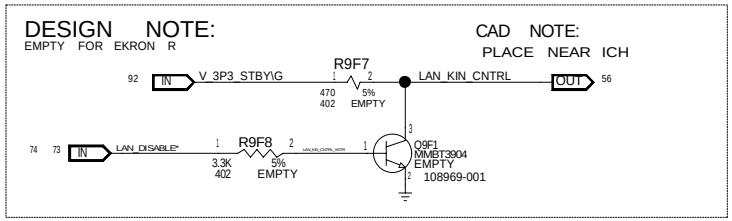
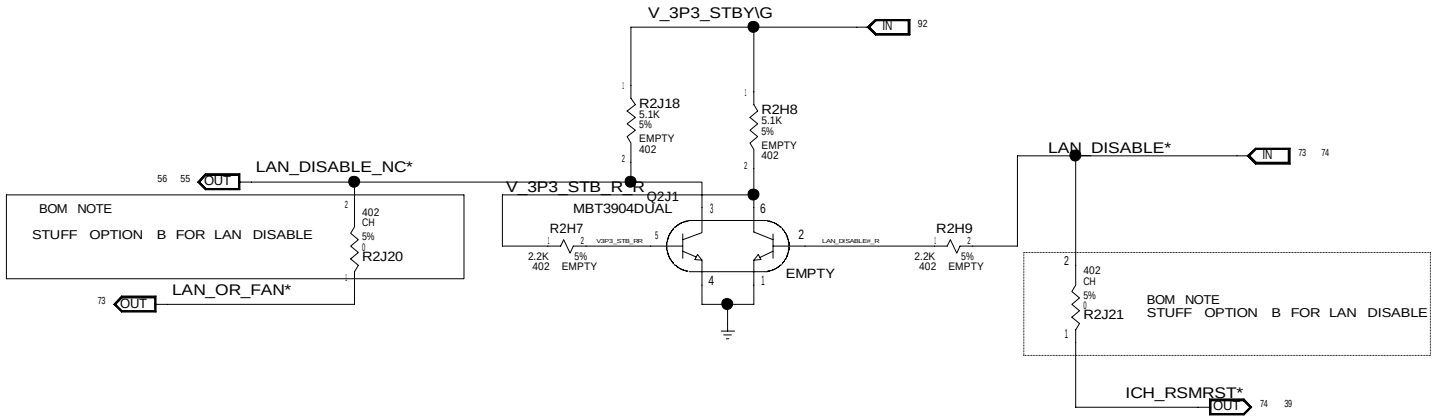




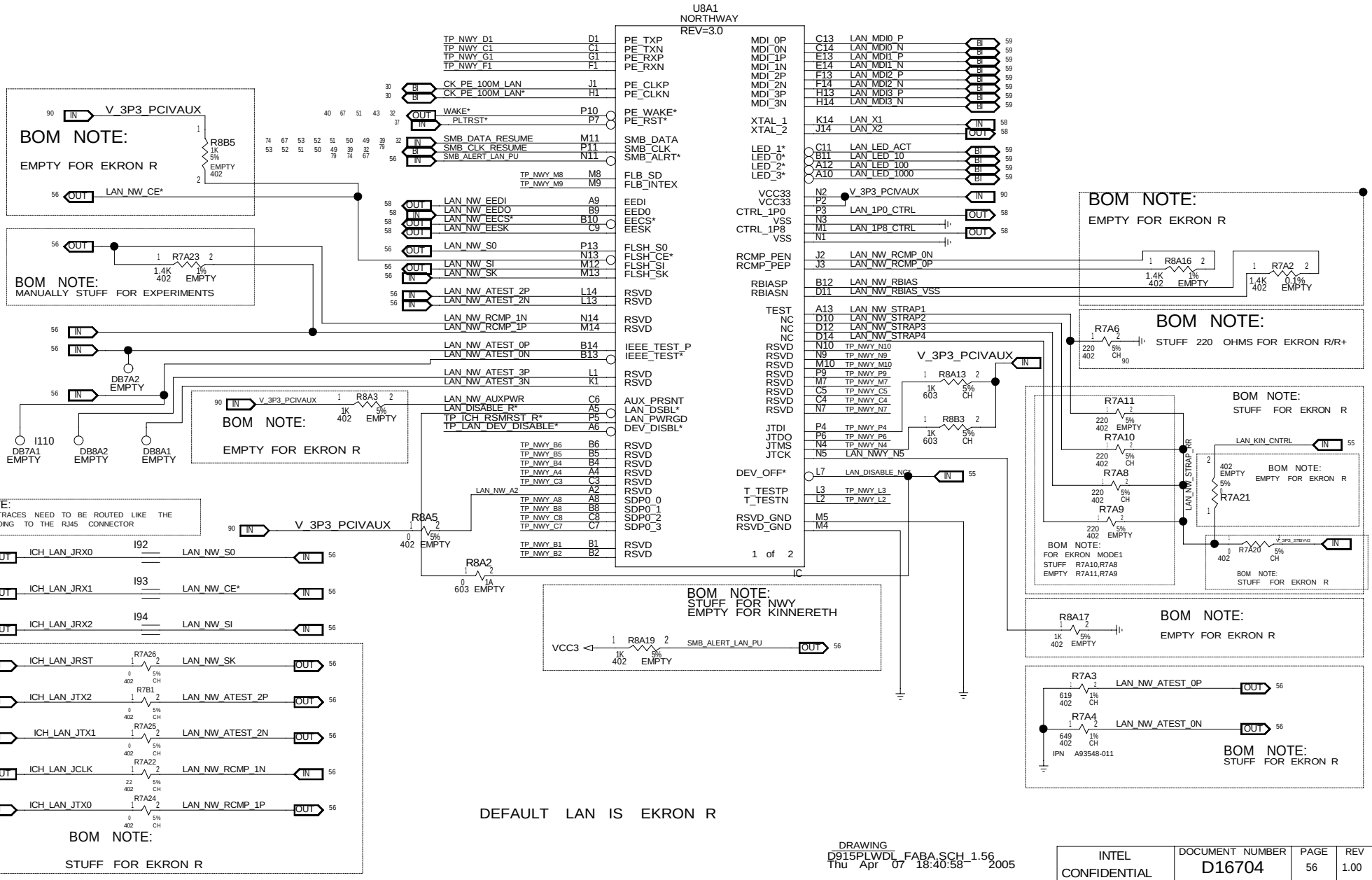




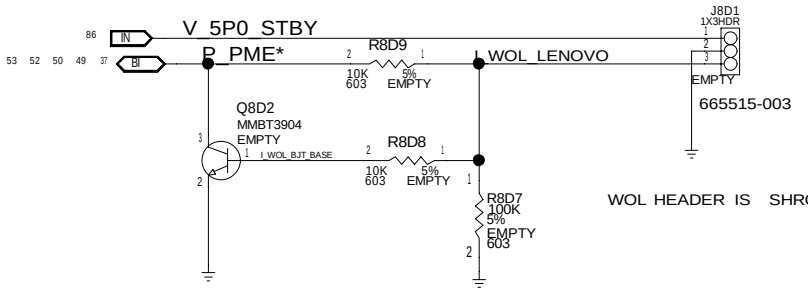


DRAWING
D915PLWDL_FABA.SCH_1.55
Thu Apr 07 15:10:17 2005

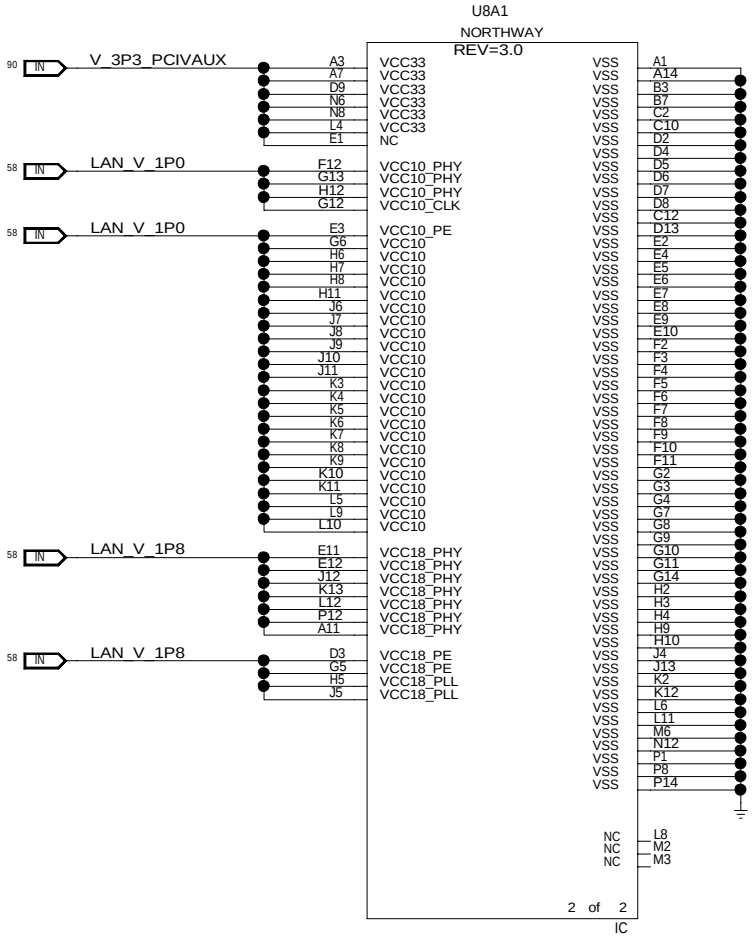
[PAGE_TITLE=ICH TO LAN CONTROL]


U8A1
NORTHWAY
REV=3.0
PE_TXP
PE_TXN
PE_RXP
PE_RXN
PE_CLKP
PE_CLKN
PE_WAKE*
PE_RST*
SMB_DATA
SMB_CLK
SMB_ALRT*
FLB_SD
FLB_INTEX
EEDI
EED0
EECS*
EESK
FLSH_S0
FLSH_CE*
FLSH_SI
FLSH_SK
RSVD
RSVD
RSVD
RSVD
IEEE_TEST_P
IEEE_TEST*
RSVD
RSVD
AUX_PRSNT
LAN_DSBL*
LAN_PWRGD
DEV_DISBL*
RSVD
RSVD
RSVD
RSVD
RSVD
RSVD
SDP0_0
SDP0_1
SDP0_2
SDP0_3
RSVD
RSVD
MDI_0P
MDI_0N
MDI_1P
MDI_1N
MDI_2P
MDI_2N
MDI_3P
MDI_3N
XTAL_1
XTAL_2
LED_1*
LED_0*
LED_2*
LED_3*
VCC33
VCC33
CTRL_1P0
VSS
CTRL_1P8
VSS
RCMP_PEN
RCMP_PEP
RBIASP
RBIASN
TEST
NC
NC
NC
RSVD
RSVD
RSVD
RSVD
RSVD
RSVD
RSVD
JTDI
JTDO
JTMS
JTCK
DEV_OFF*
T_TESTP
T_TESTN
RSVD_GND
RSVD_GND
1 of 2
IC
V_3P3_PCIVAUX
R8B5
1K
5%
EMPTY
402
BOM NOTE:
EMPTY FOR EKRON R
LAN_NW_CE*
R7A23
1.4K
1%
402
EMPTY
BOM NOTE:
MANUALLY STUFF FOR EXPERIMENTS
DB7A2
EMPTY
I110
DB7A1
EMPTY
DB8A2
EMPTY
DB8A1
EMPTY
R8A3
1K
5%
402
EMPTY
BOM NOTE:
EMPTY FOR EKRON R
CAD NOTE:
DEBUG PAD TRACES NEED TO BE ROUTED LIKE THE MDI LINE GOING TO THE RJ45 CONNECTOR
R8A5
0
402
EMPTY
R8A2
0
603
EMPTY
I92
I93
I94
ICH_LAN_JRX0
ICH_LAN_JRX1
ICH_LAN_JRX2
LAN_NW_S0
LAN_NW_CE*
LAN_NW_SI
ICH_LAN_JRST
ICH_LAN_JTX2
ICH_LAN_JTX1
ICH_LAN_JCLK
ICH_LAN_JTX0
LAN_NW_SK
LAN_NW_ATEST_2P
LAN_NW_ATEST_2N
LAN_NW_RCMP_1N
LAN_NW_RCMP_1P
R7A26
R7B1
R7A25
R7A22
R7A24
0
402
CH
22
BOM NOTE:
STUFF FOR EKRON R
BOM NOTE:
STUFF FOR NWY
EMPTY FOR KINNERETH
VCC3
R8A19
1K
5%
402
EMPTY
SMB_ALERT_LAN_PU
DEFAULT LAN IS EKRON R
LAN_MDI0_P
LAN_MDI0_N
LAN_MDI1_P
LAN_MDI1_N
LAN_MDI2_P
LAN_MDI2_N
LAN_MDI3_P
LAN_MDI3_N
LAN_X1
LAN_X2
LAN_LED_ACT
LAN_LED_10
LAN_LED_100
LAN_LED_1000
V_3P3_PCIVAUX
LAN_1P0_CTRL
LAN_1P8_CTRL
LAN_NW_RCMP_0N
LAN_NW_RCMP_0P
LAN_NW_RBIAS
LAN_NW_RBIAS_VSS
LAN_NW_STRAP1
LAN_NW_STRAP2
LAN_NW_STRAP3
LAN_NW_STRAP4
TP_NWY_N10
TP_NWY_N9
TP_NWY_M10
TP_NWY_P9
TP_NWY_M7
TP_NWY_C5
TP_NWY_C4
TP_NWY_N7
TP_NWY_P4
TP_NWY_P6
TP_NWY_N4
LAN_NWY_N5
LAN_DISABLE_NC
TP_NWY_L3
TP_NWY_L2
R8A13
R8B3
1K
603
5%
CH
BOM NOTE:
EMPTY FOR EKRON R
R8A16
1.4K
1%
402
EMPTY
R7A2
1.4K
0.1%
402
EMPTY
BOM NOTE:
STUFF 220 OHMS FOR EKRON R/R+
R7A6
220
5%
402
CH
R7A11
R7A10
R7A8
R7A9
220
402
EMPTY
BOM NOTE:
STUFF FOR EKRON R
LAN_KIN_CNTRL
R7A21
BOM NOTE:
FOR EKRON MODE1
STUFF R7A10,R7A8
EMPTY R7A11,R7A9
R7A20
BOM NOTE:
STUFF FOR EKRON R
R8A17
BOM NOTE:
EMPTY FOR EKRON R
R7A3
619
1%
LAN_NW_ATEST_0P
R7A4
649
LAN_NW_ATEST_0N
IPN A93548-011
BOM NOTE:
STUFF FOR EKRON R

LEGEND WAKE ON LAN HEADER



WOL HEADER IS SHROUDED ON ONE SIDE



[PAGE_TITLE=LAN CONTROLLER, PART 2 OF 2]

DRAWING
D915PLWDL_FABA.SCH_1.57
Wed Apr 06 22:21:18 2005

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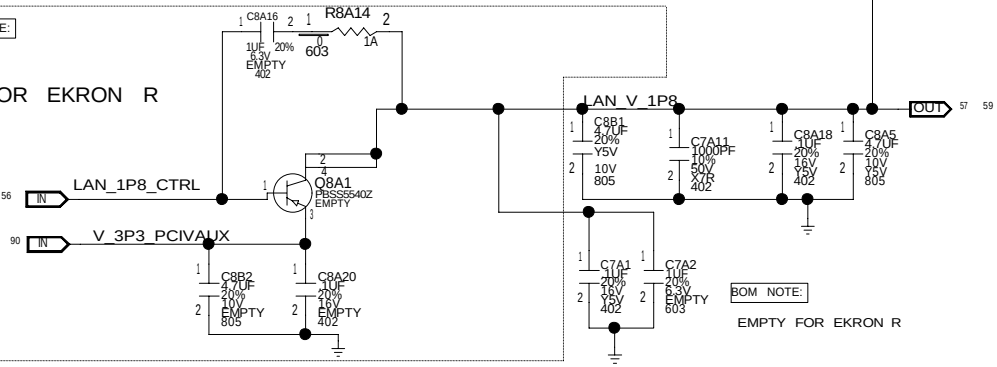
	D16704	57	1.00

VOLTAGE REGULATION - PHY

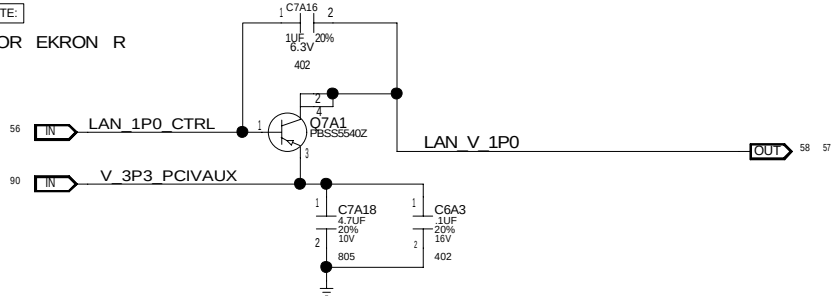
BOM NOTE:
STUFF FOR EKRON R

BOM NOTE:
EMPTY FOR EKRON R



BOM NOTE:
EMPTY FOR EKRON R

BOM NOTE:
EMPTY FOR EKRON R



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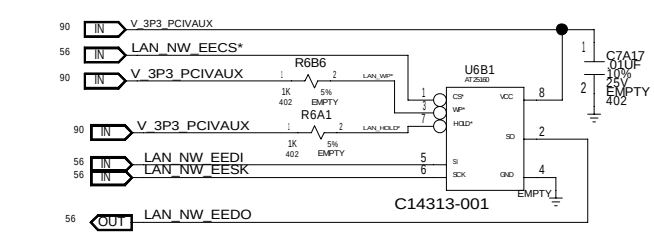
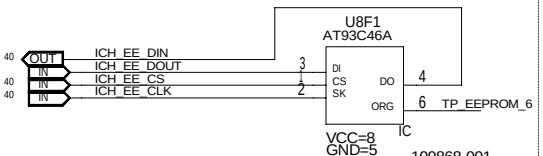
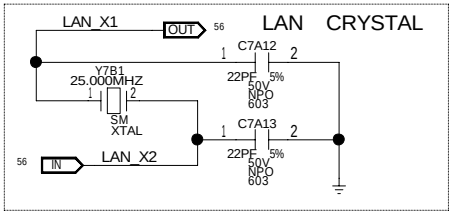




PLACEHOLDER: ICH/EKRON R EEPROM

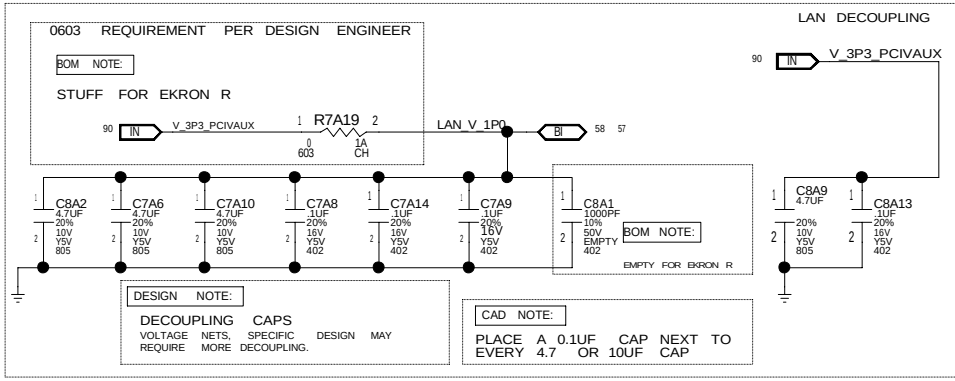
BOM NOTE:
STUFF FOR EKRON R



LAN DECOUPLING

0603 REQUIREMENT PER DESIGN ENGINEER

BOM NOTE:
STUFF FOR EKRON R



DESIGN NOTE:
DECOUPLING CAPS
VOLTAGE NETS, SPECIFIC DESIGN MAY REQUIRE MORE DECOUPLING.

CAD NOTE:
PLACE A 0.1UF CAP NEXT TO EVERY 4.7 OR 10UF CAP

DRAWING
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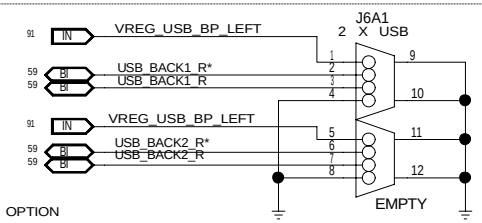
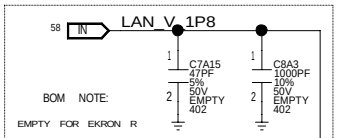
	D16704	58	1.00

CAD NOTE:

OVERLAP WITH MAGJACK FOOTPRINT
* MODEL HAS DIFFERENT PIN ORIENTTION THAN MAGJACK FOOTPRINT



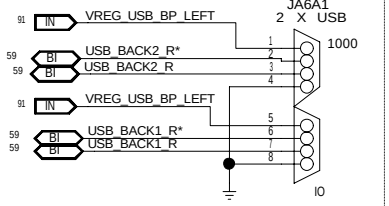
BOM NOTE:
EMPTY EXCEPT FOR USB W/NO-LAN OPTION



LAN CONNECTOR DEFAULT GIGABIT

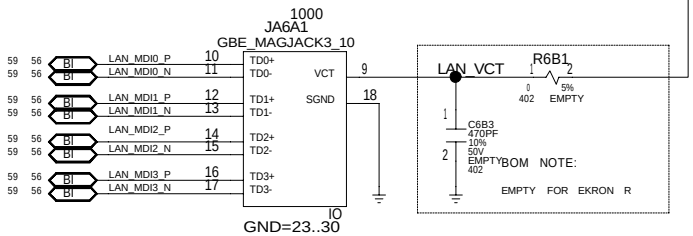
MAGJACK	SPEED LED
10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW

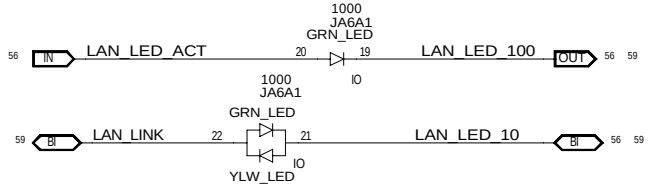
USB STACK



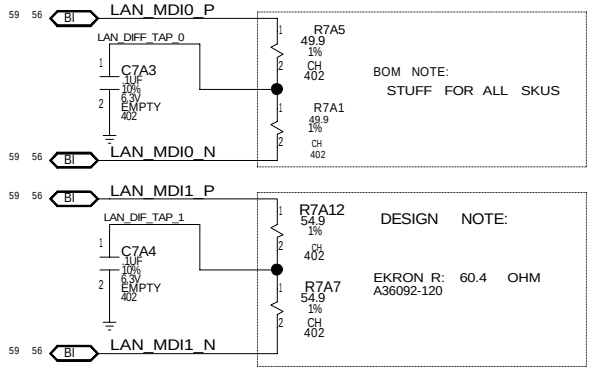
DESIGN NOTE:

USE CONNECTOR A74307-001 WITH KENAI
USE CONNECTOR A74314-001 WITH LAVON





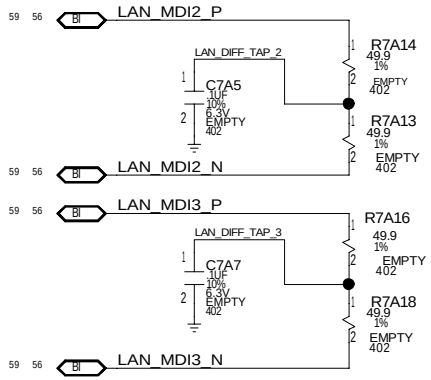
DIFFERENTIAL PAIR TERMINATONS

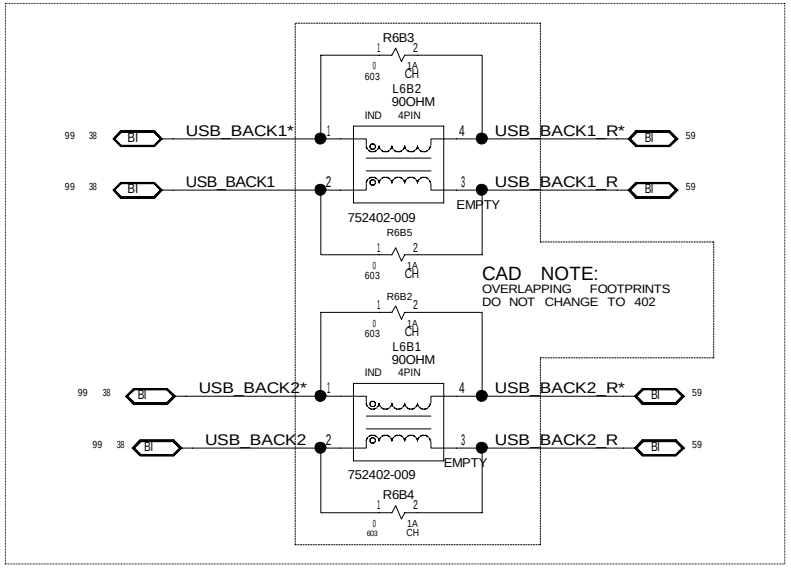


BOM NOTE:
STUFF FOR ALL SKUS

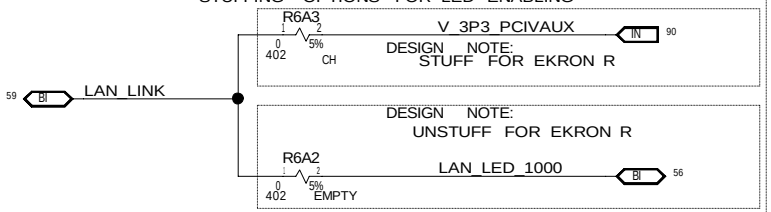
DESIGN NOTE:

EKRON R: 60.4 OHM
A36092-120



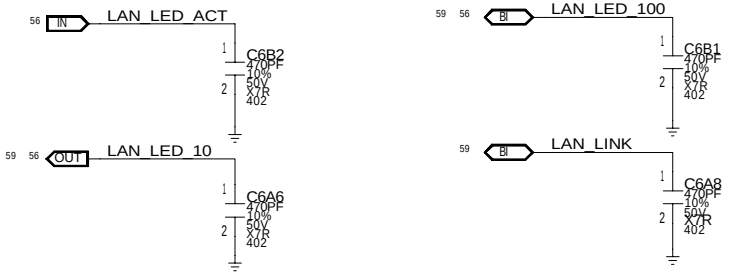


STUFFING OPTIONS FOR LED ENABLING



LED DECOUPLING

CAD NOTE:
LED CAPS SHOULD BE PLACED NEXT TO CONNECTOR



DRAWING
D915PLWDL_FABA.SCH_1.59
Wed Apr 06 22:29:04 2005

[PAGE_TITLE=LAN CONN]

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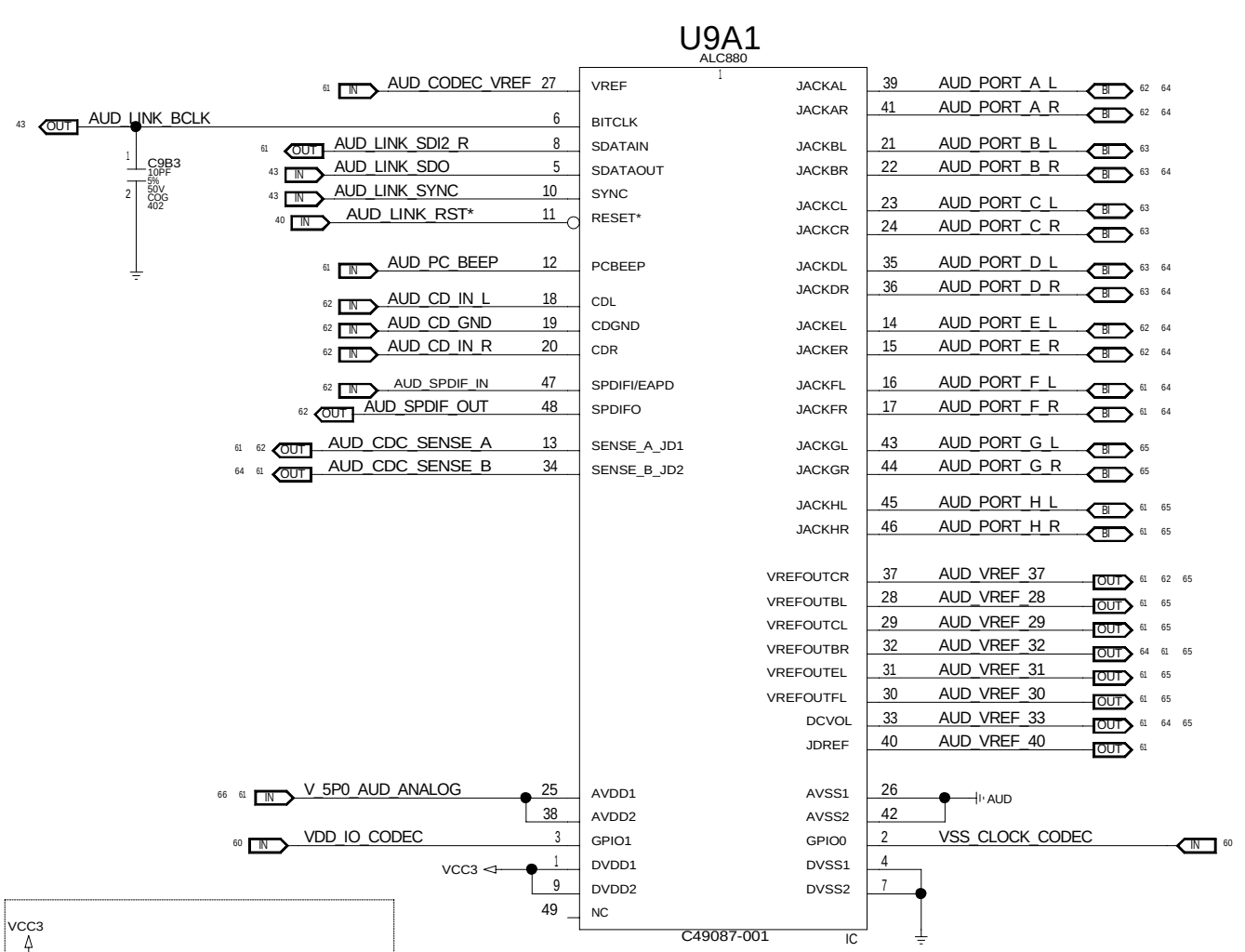
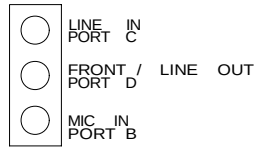
	D16704	59	1.00

DEFAULT AUDIO CODEC: AZALIA REALTEK





FACING BACK PANEL

PORT E / PORT F ON FRONT PANEL

DESIGN NOTE:

AZALIA:

CMEDIA: CMI9880
REALTEK: ALC880,ALC860

AC97:

CMEDIA: CMI9762+,9780
REALTEK: ALC650,655,658,850, ALC202A

AUDIO CODEC

DRAWING D915PLWDL_FABA.SCH_1.60
Wed Apr 06 22:28:59 2005

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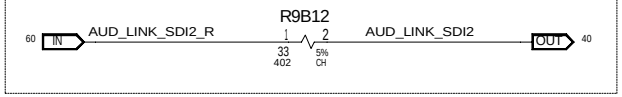
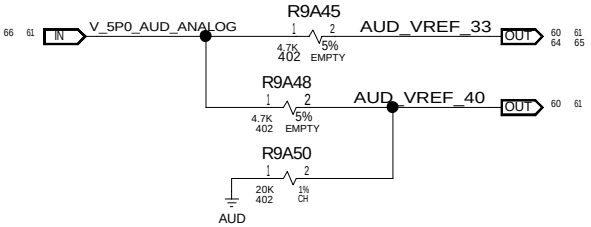
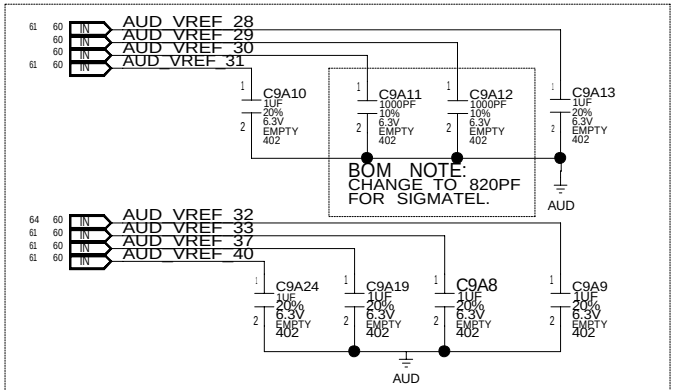
	D16704	60	1.00

CAD NOTE:
PLACE NEAR ICH PINS

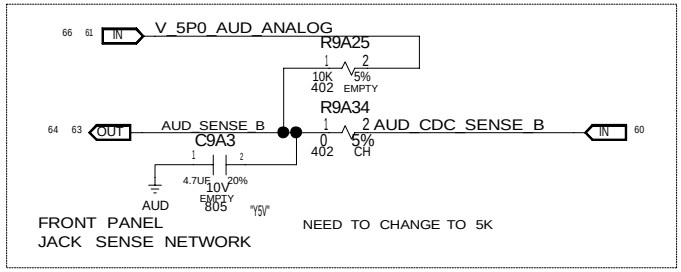






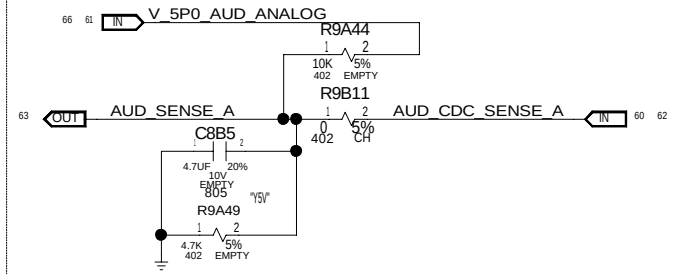
CAD NOTE:
PLACE NEAR EACH VREF PIN

VREF DECOUPLING

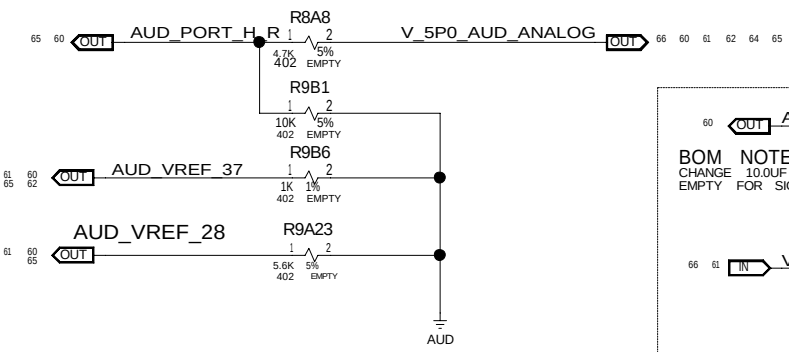


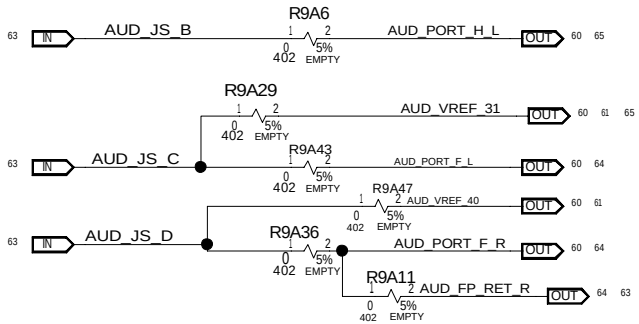
FRONT PANEL
JACK SENSE NETWORK

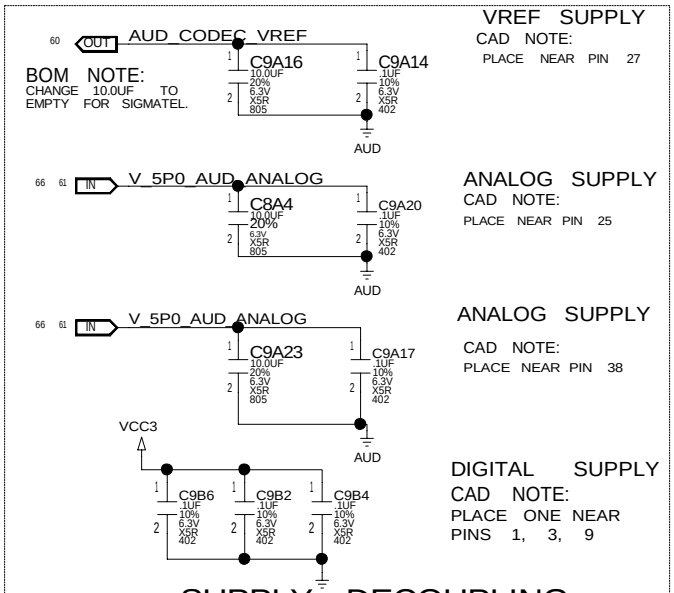
NEED TO CHANGE TO 5K



BACK PANEL
JACK SENSE NETWORK







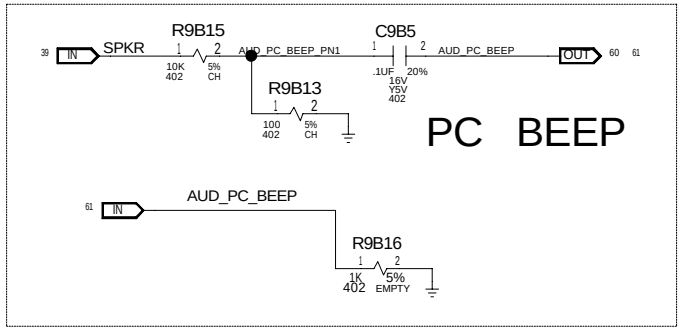
VREF SUPPLY
CAD NOTE:
PLACE NEAR PIN 27

ANALOG SUPPLY
CAD NOTE:
PLACE NEAR PIN 25

ANALOG SUPPLY
CAD NOTE:
PLACE NEAR PIN 38

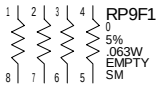
DIGITAL SUPPLY
CAD NOTE:
PLACE ONE NEAR
PINS 1, 3, 9

SUPPLY DECOUPLING



PC BEEP

DECOUPLING AND JACK SENSE



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D915PLWDL_FABA.SCH_1.61
Thu Apr 07 09:23:42 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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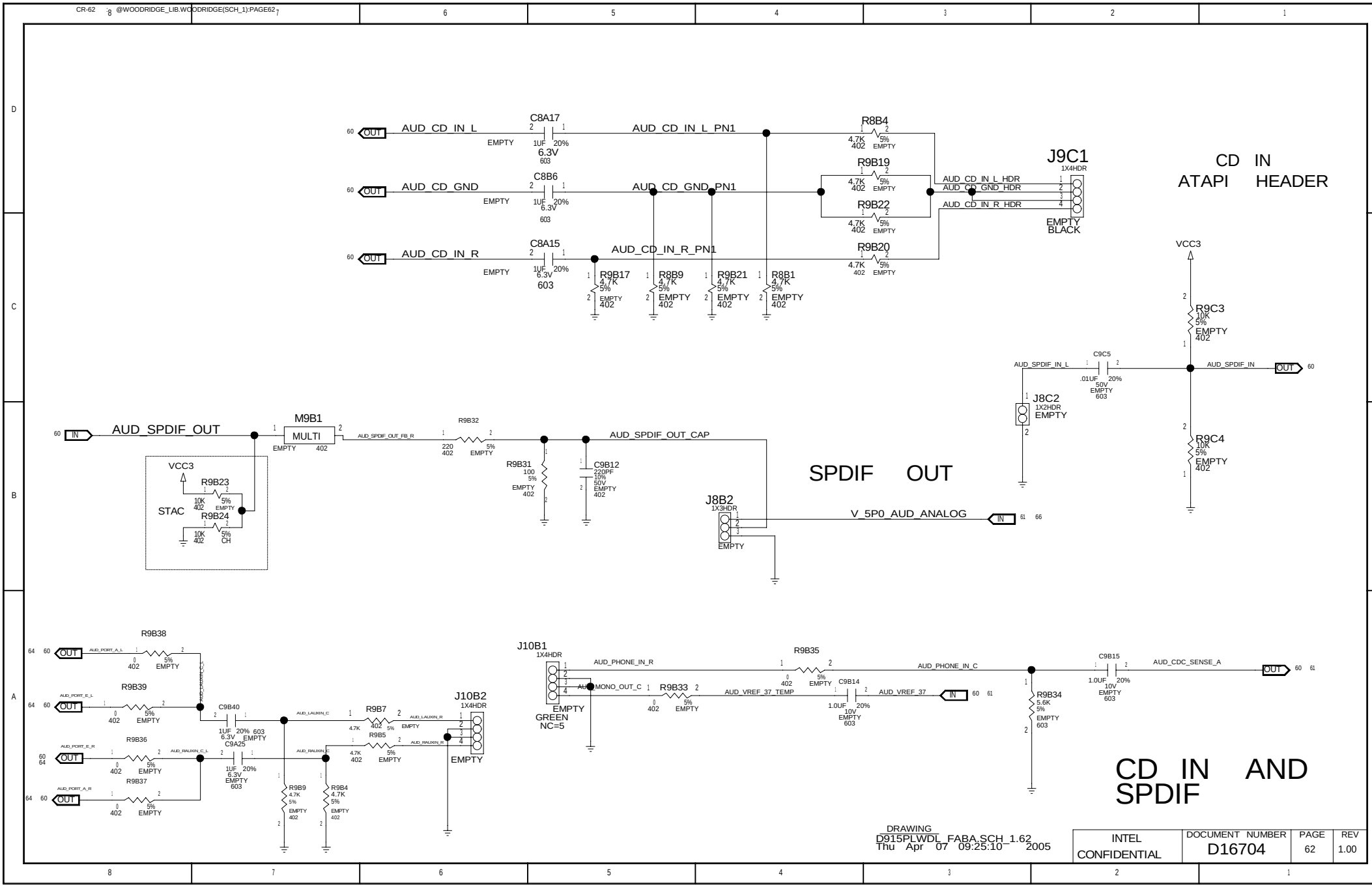

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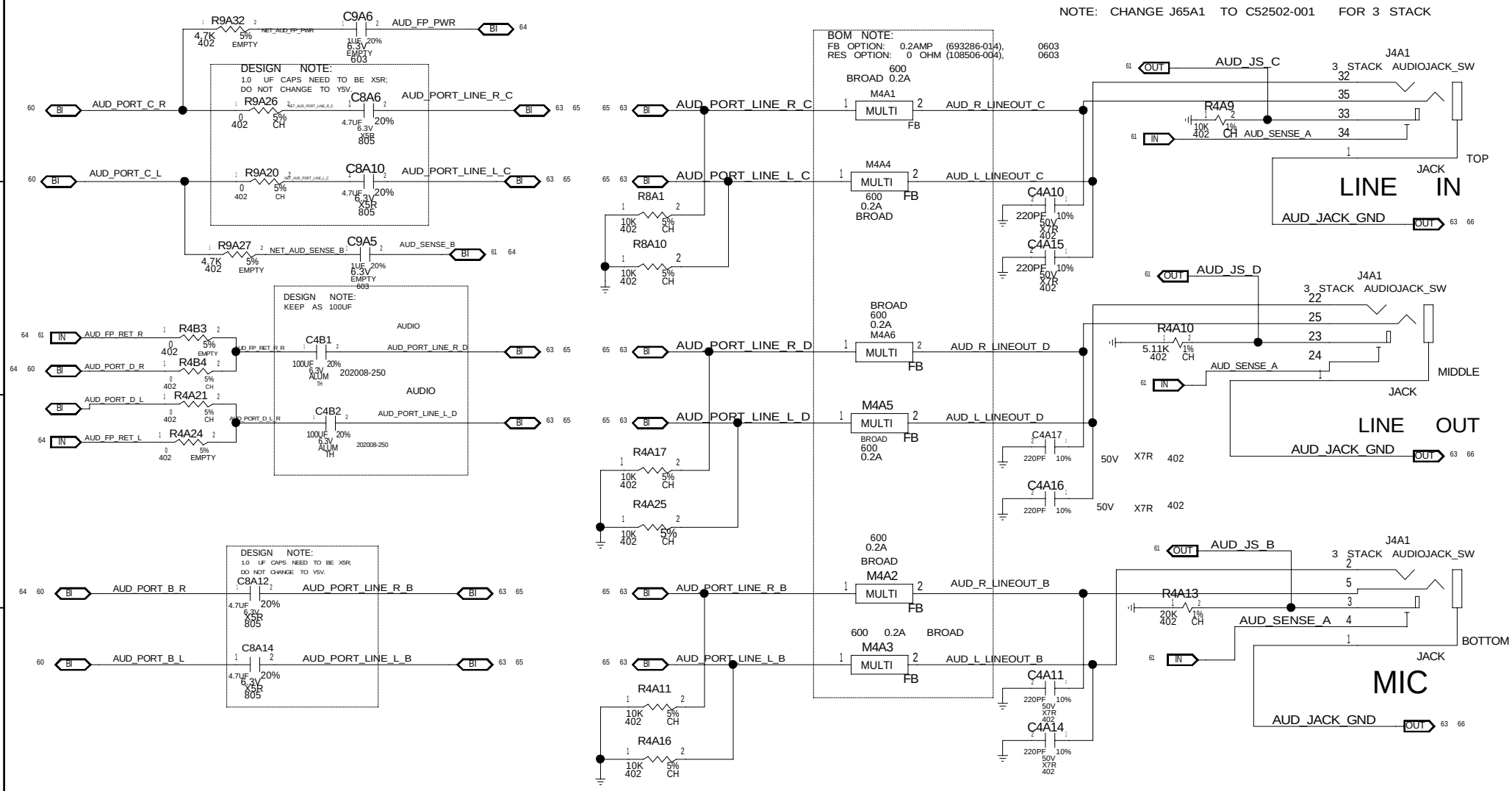
D915PLWDL_FABA.SCH_1.62
Thu Apr 07 09:25:10 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	62	1.00

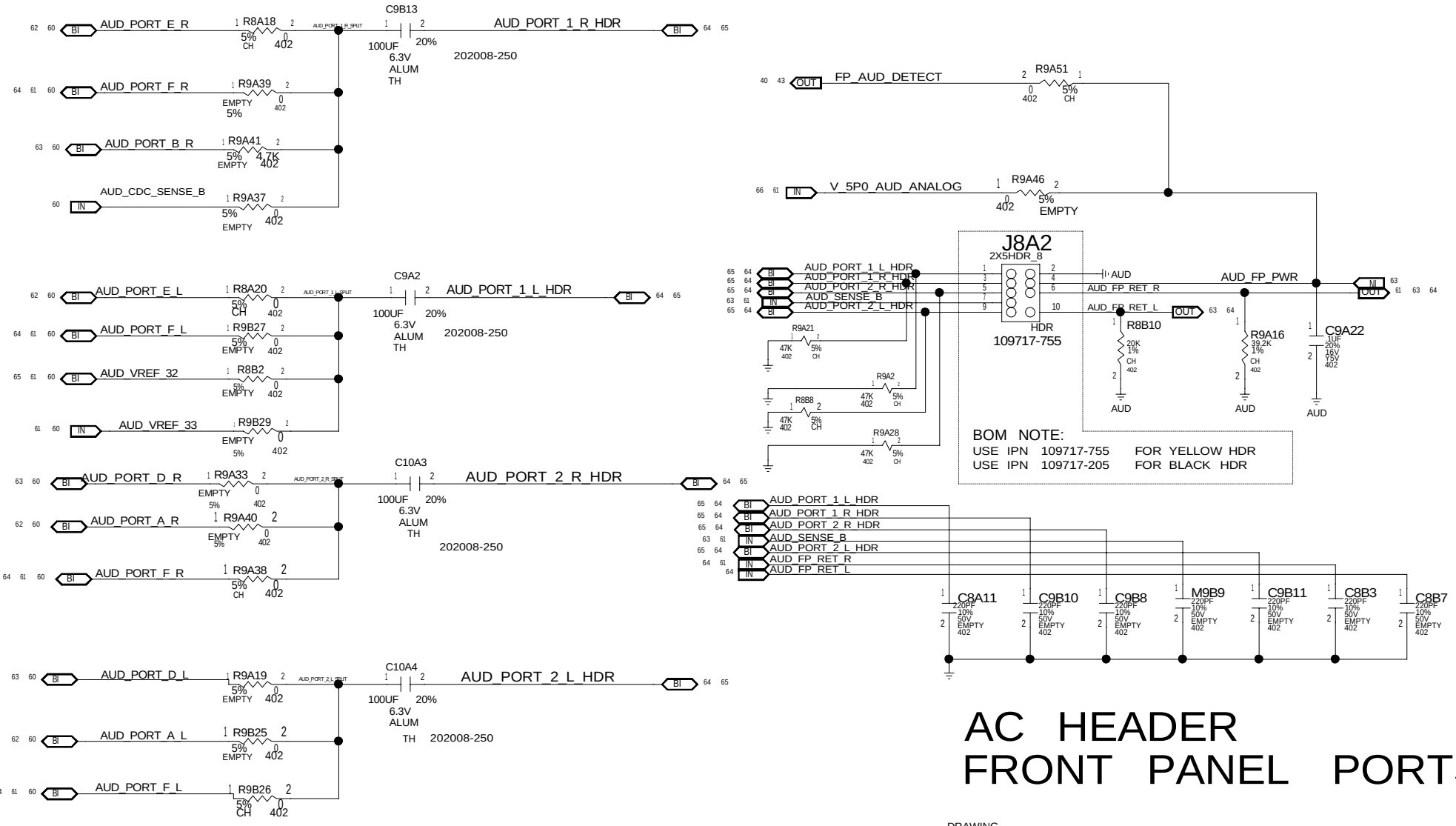


BACK PANEL PORTS

AUDIO BACK PANEL

DRAWING
D915PLWDL_FABA.SCH_1.63
Thu Apr 07 09:27:25 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	63	1.00

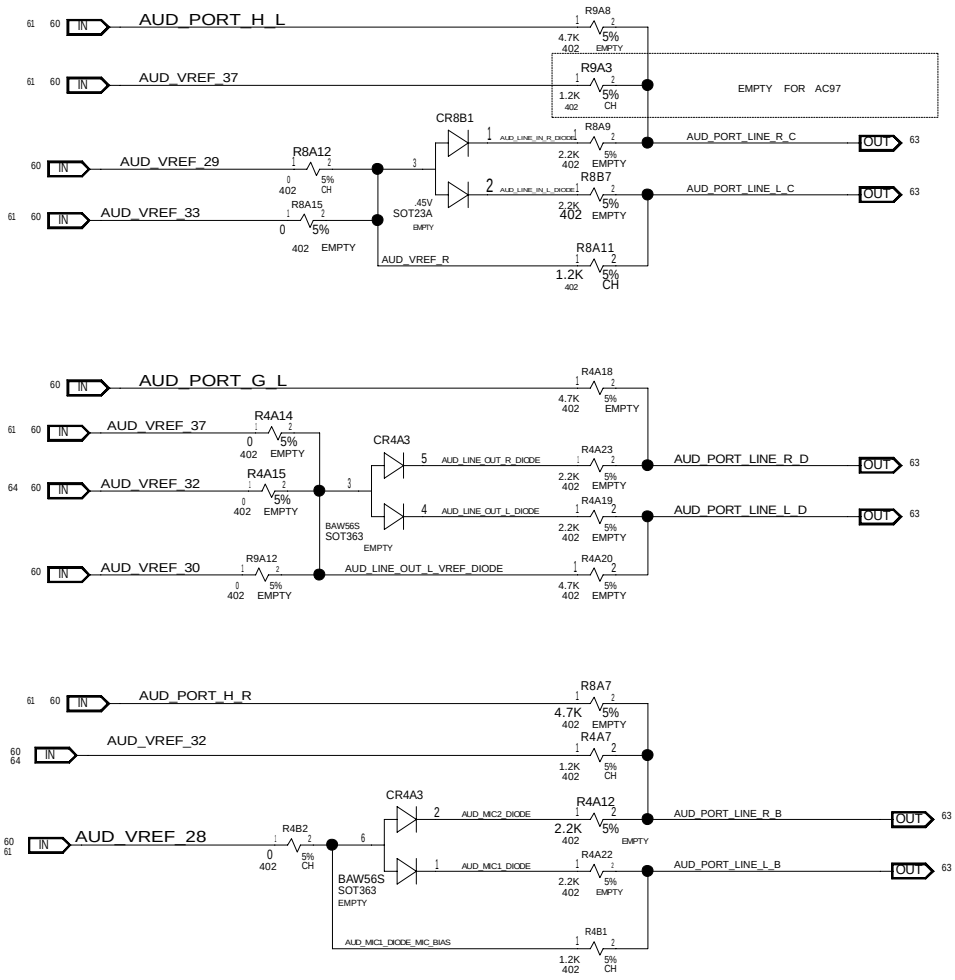


AC HEADER
FRONT PANEL PORTS

DRAWING
D915PLWDL_FABA.SCH_1.64
Thu Apr 07 16:14:07 2005

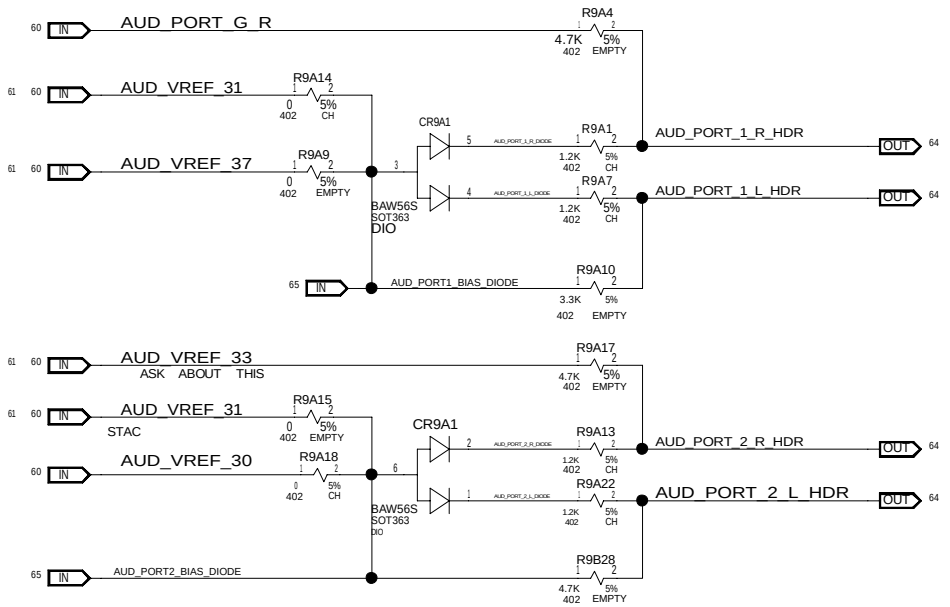
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	64	1.00

3 STACK 1

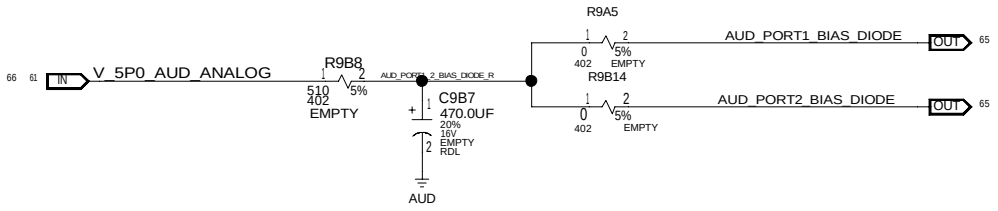


TERMINATION/PULL-UPS

FRONT PANEL



TERMINATION/PULL-UPS

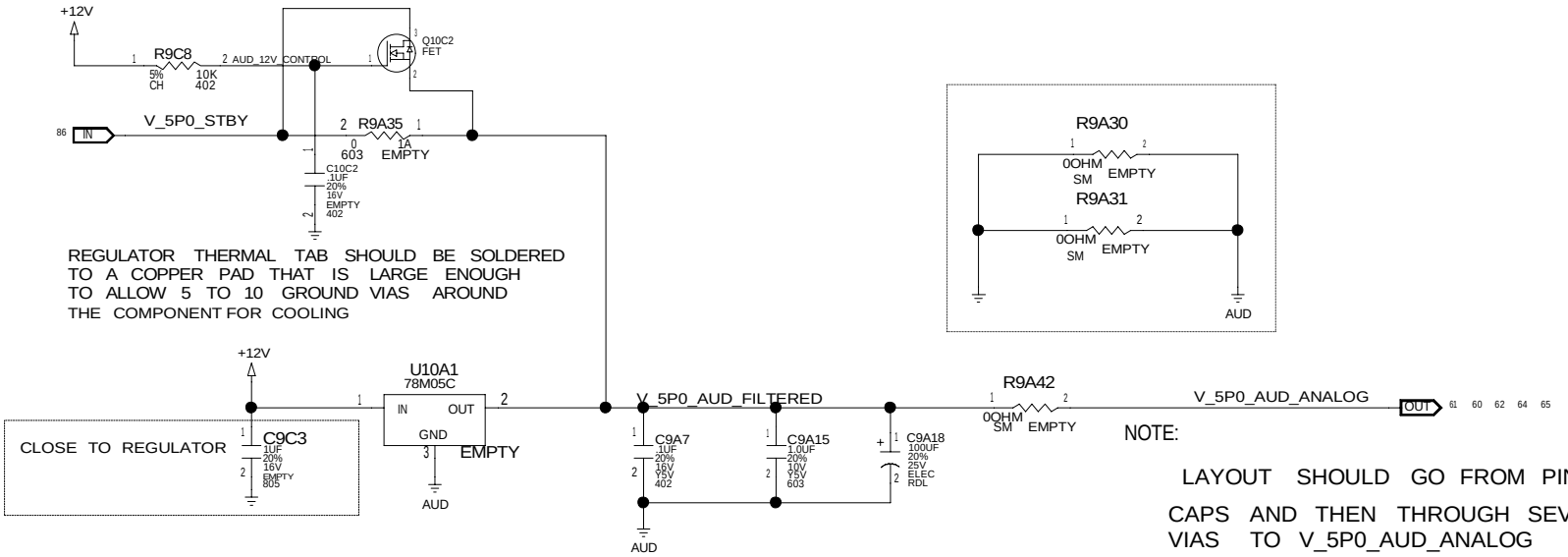


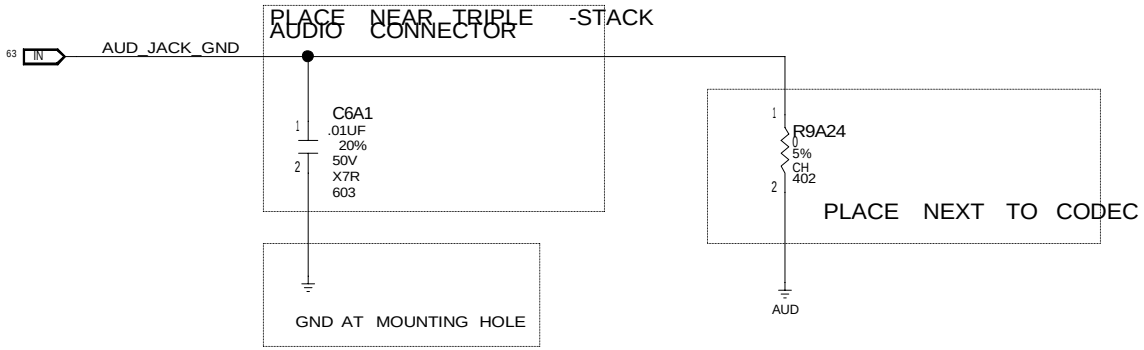
VREF NETWORKS

DRAWING
D915PLWDL_FABA.SCH_1.65
Thu Apr 07 09:30:05 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	65	1.00

PLACE IN TOP LEFT CORNER OF BOARD





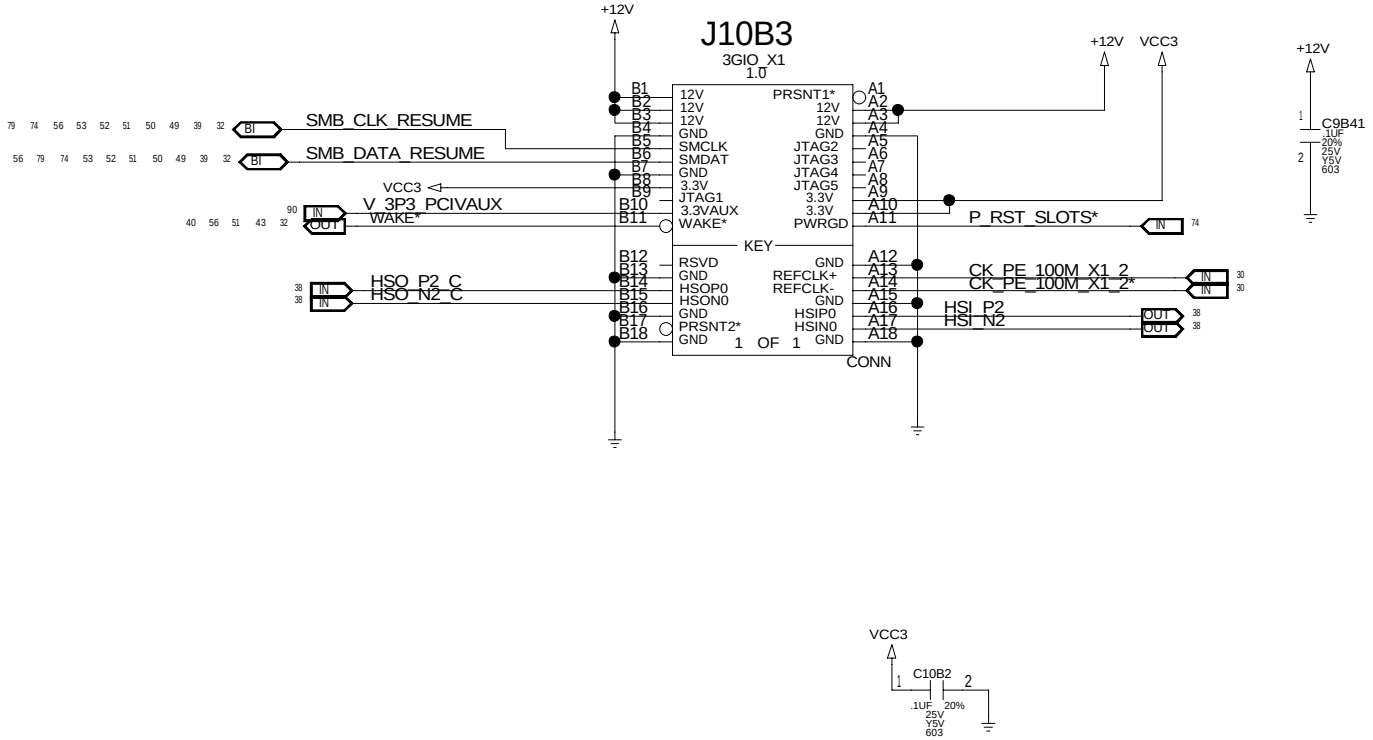
DRAWING
D915PLWDL_FABA.SCH_1.66
Thu Apr 07 09:31:17 2005

[PAGE_TITLE=AUDIO_VREG]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	66	1.00

BACK PANEL SLOT 3
PCI EXPRESS X1 SLOT 2

BOM NOTE:
USE C55845-001
FOR X1 CONN



[TITLE=PCIE_X1_CONN_2]

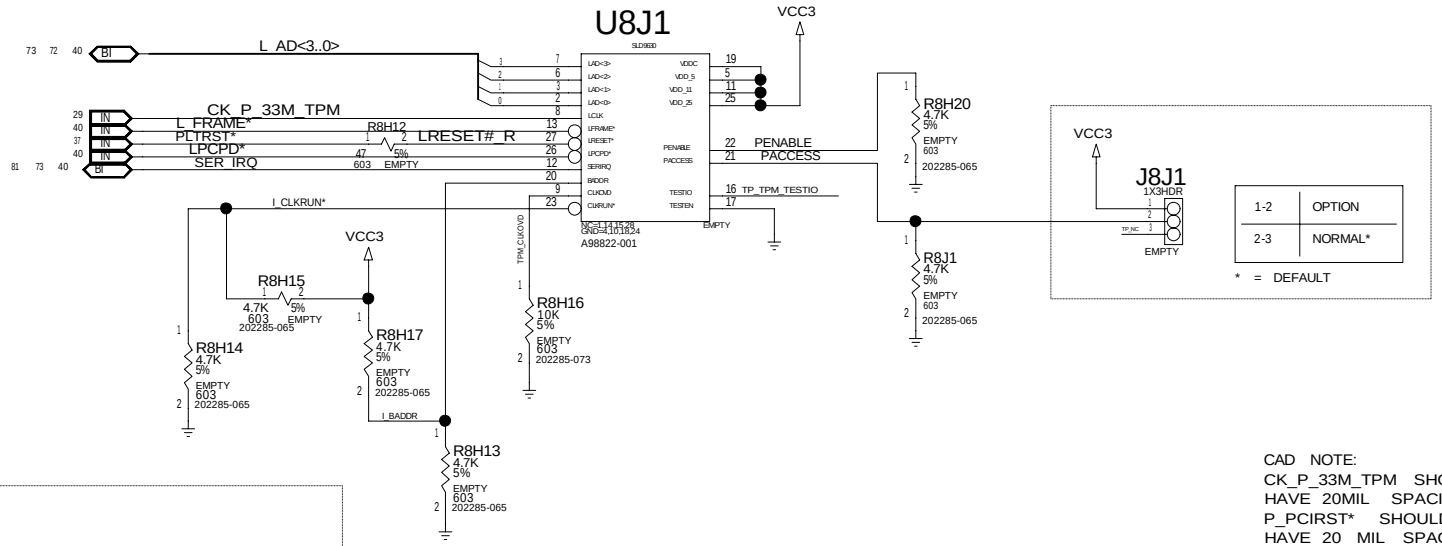
DRAWING
D915PLWDL_FABA.SCH_1.67
Wed Apr 06 23:06:25 2005

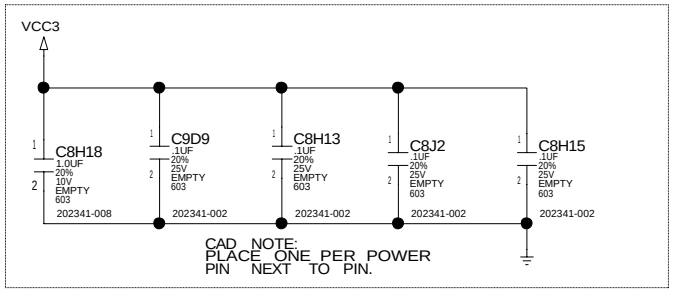
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	67	1.00

BLANK

BLANK

SECURITY: TPM (TRUSTED PLATFORM MODULE)

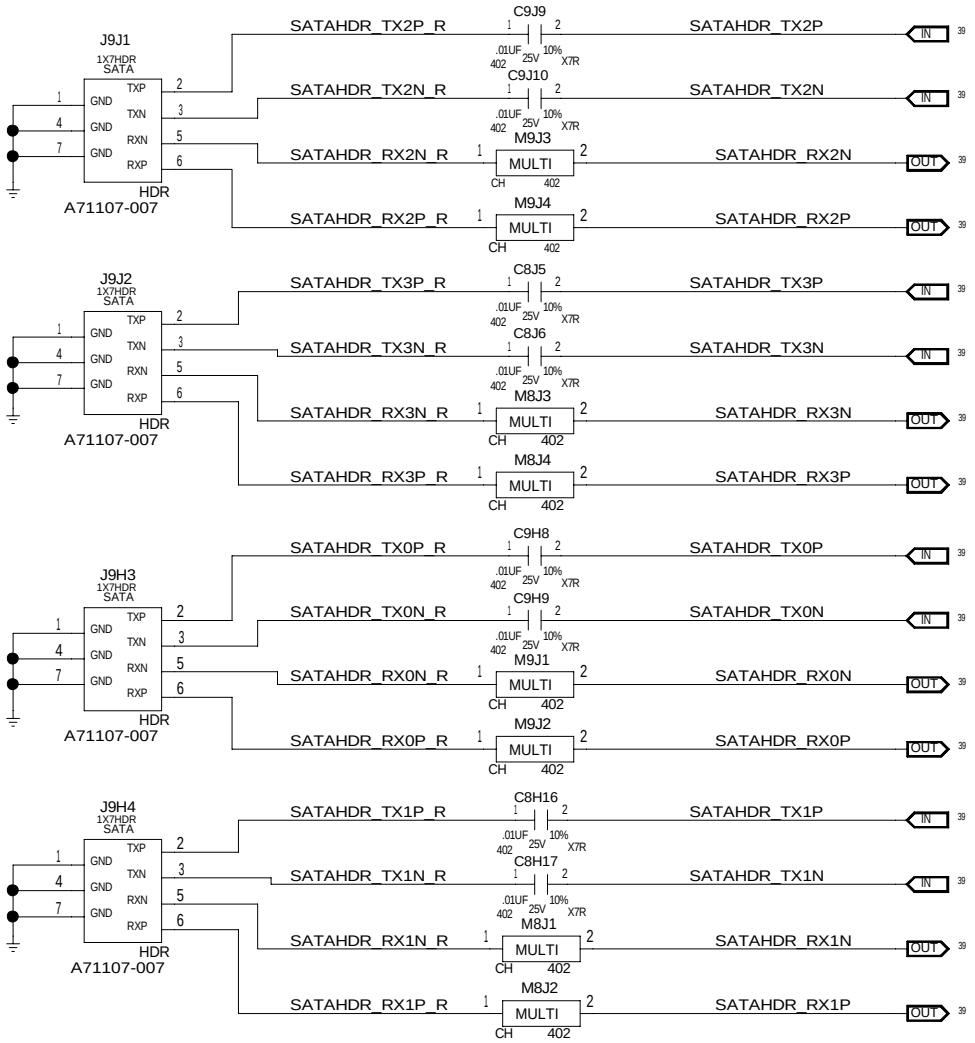




CAD NOTE:
CK_P_33M_TPM SHOULD HAVE 20MIL SPACING
P_PCIRST* SHOULD HAVE 20 MIL SPACING
LAD<3..0> HAS 5 MIL SPACING BETWEEN OTHER LAD SIGNALS, BUT 10 MILS TO ALL OTHER SIGNALS.

[PAGE_TITLE=TPM (TRUSTED PLATFORM MODULE)]

BOM NOTE:
FOR M-SITES, USE A36096-008 (.01UF, 0402)



[PAGE_TITLE=SATA CONNECTORS]

DRAWING
D915PLWDL_FABA.SCH_1.71
Thu Apr 07 16:25:09 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	71	1.00

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY

* DEFAULT JUMPER SETTING

CONFIGURE= SAFE MODE

BOM NOTE:
USING IPN C55248-001

U8J2
FWH

L_AD<3..0>

PWRGD_3V — R8H11 1K 603 5% CH — FWH_WP_C

J8H1 1X2HDR EMPTY

R8J5 4.7K 402 5% CH — FWH_WP*

R8J6 4.7K 402 5% CH — FWH_TBL*

TP_FWH_29

PLTRST* — R8H19 47 402 5% CH — FWH_RST*

CK_P_33M_FWH

L_FRAME*

+12V — R7H16 1K 5% CH 402 — PN201W — Q7H2 FET

VCC3

FWH_VPP

C8H19 1UF 20% 25V Y5V 603

VCC3 — C8H20 1UF 20% 25V EMPTY 603; C7H11 1UF 20% 25V Y5V 603; C7J1 1UF 20% 25V Y5V 603

FIRMWARE HUB DECOUPLING

FWH			
WP	7	FWH3	17
TBL	8	FWH2	15
IC	29	FWH1	14
RST	2	FWH0	13
CLK	31	DQ4/RFU	18 TP_FWH_13
FWH4	23	DQ5/RFU	19 TP_FWH_19
VPP	1	DQ6/RFU	20 TP_FWH_20
VCCA/NC	27	DQ7/RFU	21 TP_FWH_21
VCC	32	RY/BY/RFU	22 TP_FWH_22
VCC	25	FGPI4	30 PN_FWH_GPI4
GNDA/NC	28	FGPI3	3 PN_FWH_GPI3
GND	16	FGPI2	4 BOARDID<5..0>
GND	26	FGPI1	5 FWH_GPI1_R
		FGPI0	6 GPIO_DMA66_DETECT_PRI
		INIT	24 ICH_INIT_33V
		ID3	9 TP_FWH_9
		ID2	10 TP_FWH_10
		ID1	11 TP_FWH_11
		ID0	12 TP_FWH_12

IC

J7J2 JUMPER — EMPTY — ALWAYS EMPTY MFG MODE PADS

R8J8 4.7K 5% CH 402

R8J13 1K 5% CH 402 — VCC3

RECOVERY_CONFIGURE_PULLUP — SPKR

J8J4 1X3HDR HDR

BOM NOTE:
FOR YELLOW JUMPER
USE IPN 634479-005

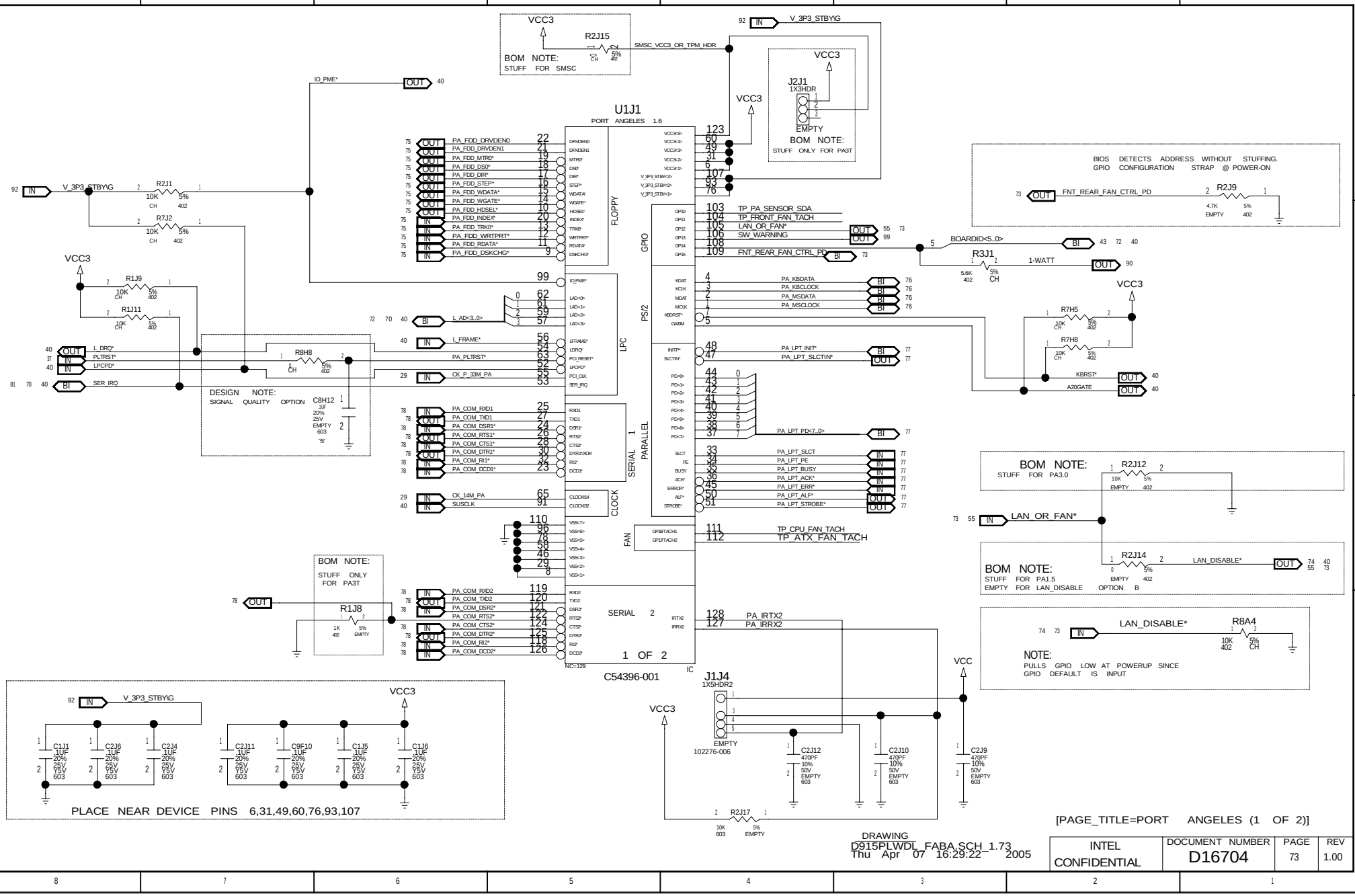
R8J4 4.7K 5% CH 402 — VCC3

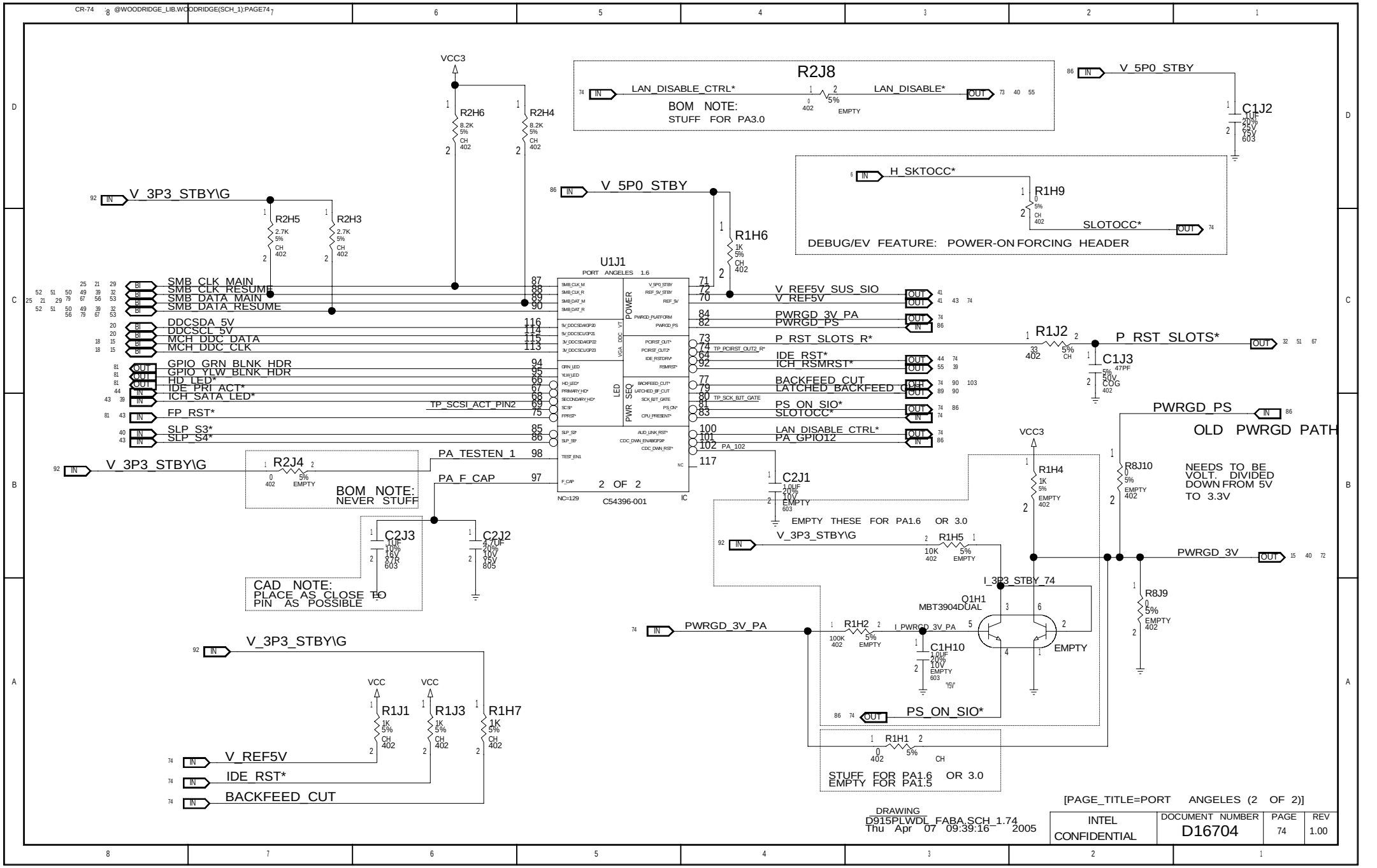
R7H13 0 402 5% EMPTY — BAT_WARN

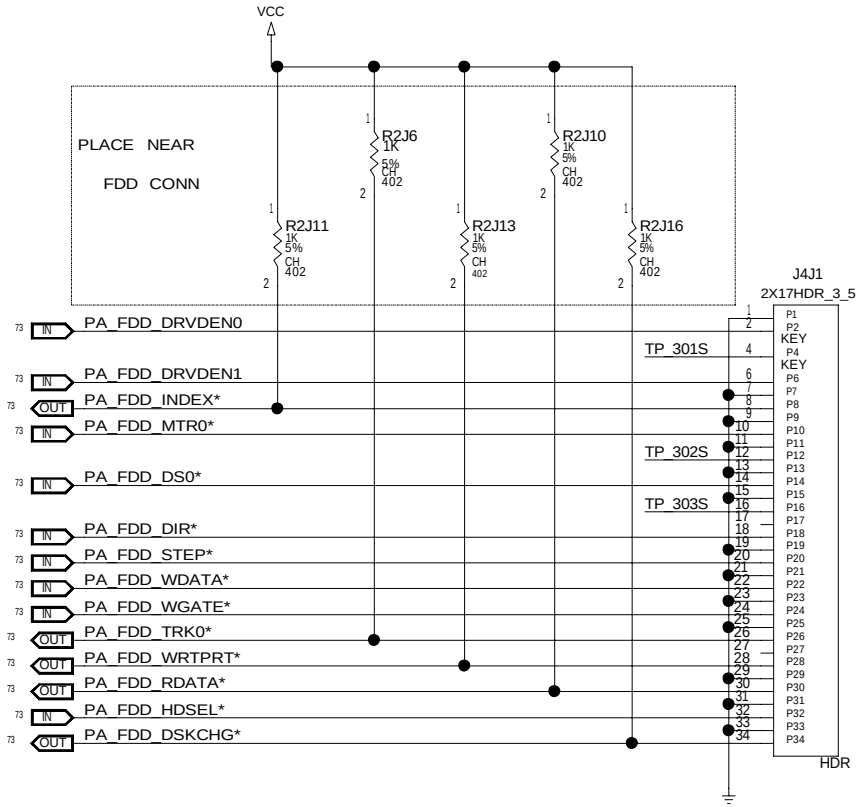
R7H15 20K 5% CH 402

[PAGE_TITLE=FIRMWARE HUB]

DRAWING
D915PLWDL_FABA.SCH_1.72
Thu Apr 07 09:34:14 2005


CR-73 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE73
U1J1
PORT ANGELES 1.6
FLOPPY
GPIO
PS/2
LPC
SERIAL 1
PARALLEL
CLOCK
FAN
SERIAL 2
1 OF 2
C54396-001
IC
NC=129
V_3P3_STBYG
VCC3
VCC
SMSC_VCC3_OR_TPM_HDR
BOM NOTE:
STUFF FOR SMSC
J2J1
1X3HDR
EMPTY
BOM NOTE:
STUFF ONLY FOR PAST
IO_PME*
L_AD<3..0>
L_FRAME*
L_DRQ*
PLTRST1*
LPCPD*
SER_IRQ
CK_P_33M_PA
DESIGN NOTE:
SIGNAL QUALITY OPTION
C8H12
PA_FDD_DRVDEN0
PA_FDD_DRVDEN1
PA_FDD_MTR0*
PA_FDD_DS0*
PA_FDD_DIR*
PA_FDD_STEP*
PA_FDD_WDATA*
PA_FDD_WGATE*
PA_FDD_HDSEL*
PA_FDD_INDEX*
PA_FDD_TRK0*
PA_FDD_WRTPRT*
PA_FDD_RDATA*
PA_FDD_DSKCHG*
TP_PA_SENSOR_SDA
TP_FRONT_FAN_TACH
LAN_OR_FAN*
SW_WARNING
FNT_REAR_FAN_CTRL_PD
PA_KBDATA
PA_KBCLOCK
PA_MSDATA
PA_MSCLOCK
PA_LPT_INIT*
PA_LPT_SLCTIN*
PA_LPT_PD<7..0>
PA_LPT_SLCT
PA_LPT_PE
PA_LPT_BUSY
PA_LPT_ACK*
PA_LPT_ERR*
PA_LPT_ALF*
PA_LPT_STROBE*
TP_CPU_FAN_TACH
TP_ATX_FAN_TACH
BOARDID<5..0>
1-WATT
KBRST*
A20GATE
BIOS DETECTS ADDRESS WITHOUT STUFFING.
GPIO CONFIGURATION STRAP @ POWER-ON
BOM NOTE:
STUFF FOR PA3.0
LAN_DISABLE*
BOM NOTE:
STUFF FOR PA1.5
EMPTY FOR LAN_DISABLE OPTION B
NOTE:
PULLS GPIO LOW AT POWERUP SINCE
GPIO DEFAULT IS INPUT
BOM NOTE:
STUFF ONLY
FOR PA3T
R1J8
PA_COM_RXD1
PA_COM_TXD1
PA_COM_DSR1*
PA_COM_RTS1*
PA_COM_CTS1*
PA_COM_DTR1*
PA_COM_RI1*
PA_COM_DCD1*
PA_COM_RXD2
PA_COM_TXD2
PA_COM_DSR2*
PA_COM_RTS2*
PA_COM_CTS2*
PA_COM_DTR2*
PA_COM_RI2*
PA_COM_DCD2*
PA_IRTX2
PA_IRRX2
J1J4
1X5HDR2
102276-006
PLACE NEAR DEVICE PINS 6,31,49,60,76,93,107
DRAWING
D915PLWDL_FABA.SCH_1.73
Thu Apr 07 16:29:22 2005
[PAGE_TITLE=PORT ANGELES (1 OF 2)]
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 73
REV 1.00


CR-74 :8 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE74 7
R2J8
LAN_DISABLE_CTRL*
LAN_DISABLE*
BOM NOTE:
STUFF FOR PA3.0
V_5P0_STBY
C1J2
H_SKTOCC*
R1H9
SLOTOCC*
DEBUG/EV FEATURE: POWER-ON FORCING HEADER
VCC3
R2H6
R2H4
V_3P3_STBY\G
R2H5
R2H3
V_5P0_STBY
R1H6
U1J1
PORT ANGELES 1.6
SMB_CLK_MAIN
SMB_CLK_RESUME
SMB_DATA_MAIN
SMB_DATA_RESUME
DDCSDA_5V
DDCSCL_5V
MCH_DDC_DATA
MCH_DDC_CLK
GPIO_GRN_BLNK_HDR
GPIO_YLW_BLNK_HDR
HD_LED*
IDE_PRI_ACT*
ICH_SATA_LED*
FP_RST*
SLP_S3*
SLP_S4*
TP_SCSI_ACT_PIN2
V_REF5V_SUS_SIO
V_REF5V
PWRGD_3V_PA
PWRGD_PS
P_RST_SLOTS_R*
IDE_RST*
ICH_RSMRST*
BACKFEED_CUT
LATCHED_BACKFEED_CUT
PS_ON_SIO*
SLOTOCC*
LAN_DISABLE_CTRL*
PA_GPIO12
PA_102
R1J2
P_RST_SLOTS*
C1J3
PWRGD_PS
OLD PWRGD PATH
NEEDS TO BE VOLT. DIVIDED DOWN FROM 5V TO 3.3V
R8J10
R1H4
R1H5
PWRGD_3V
R8J9
I_3P3_STBY_74
Q1H1
MBT3904DUAL
PWRGD_3V_PA
R1H2
I_PWRGD_3V_PA
C1H10
PS_ON_SIO*
R1H1
STUFF FOR PA1.6 OR 3.0
EMPTY FOR PA1.5
R2J4
PA_TESTEN_1
PA_F_CAP
BOM NOTE:
NEVER STUFF
C2J3
C2J2
CAD NOTE:
PLACE AS CLOSE TO PIN AS POSSIBLE
C2J1
EMPTY THESE FOR PA1.6 OR 3.0
V_3P3_STBY\G
R1J1
R1J3
R1H7
V_REF5V
IDE_RST*
BACKFEED_CUT
2 OF 2
C54396-001
NC=129
IC
DRAWING
D915PLWDL_FABA.SCH_1.74
Thu Apr 07 09:39:16 2005
[PAGE_TITLE=PORT ANGELES (2 OF 2)]
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 74
REV 1.00



[PAGE_TITLE=FDD CONN]

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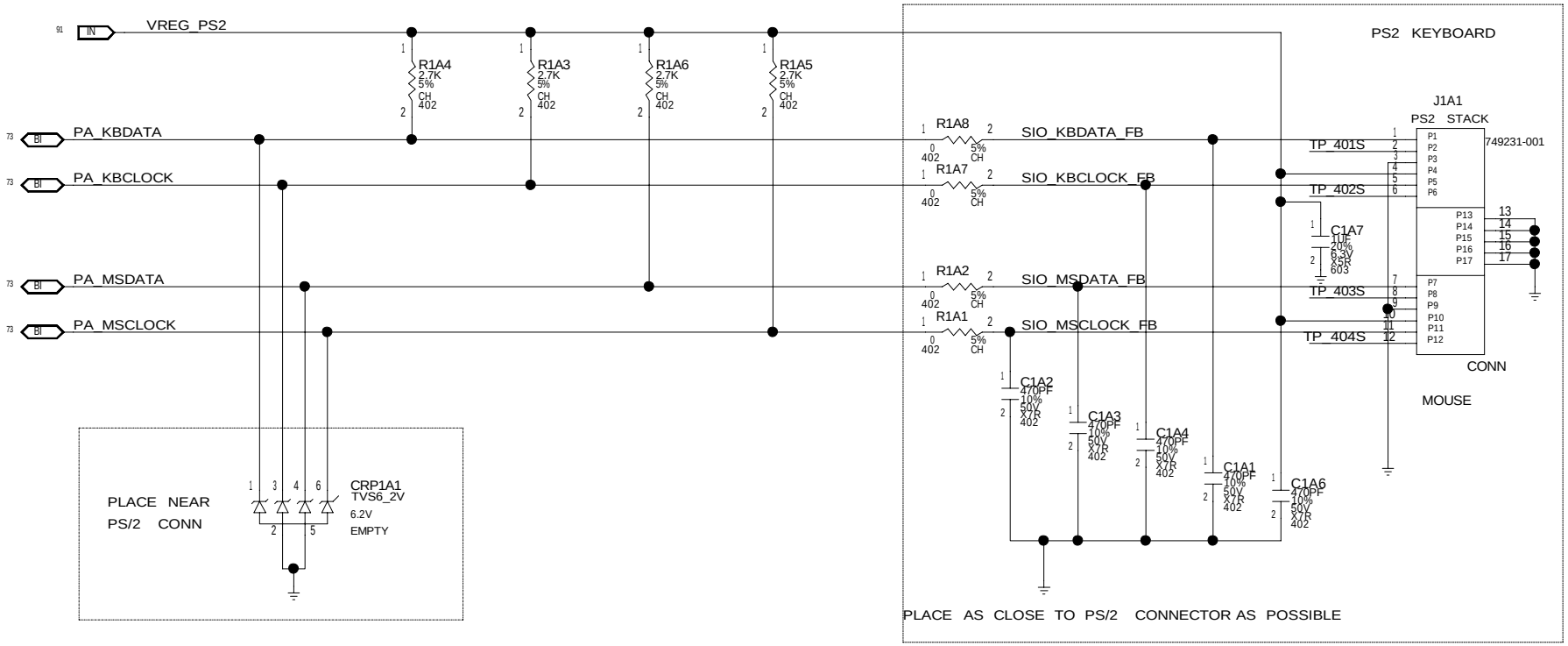
D915PLWDL_FABA.SCH_1.75
Thu Apr 07 09:39:25 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	75	1.00

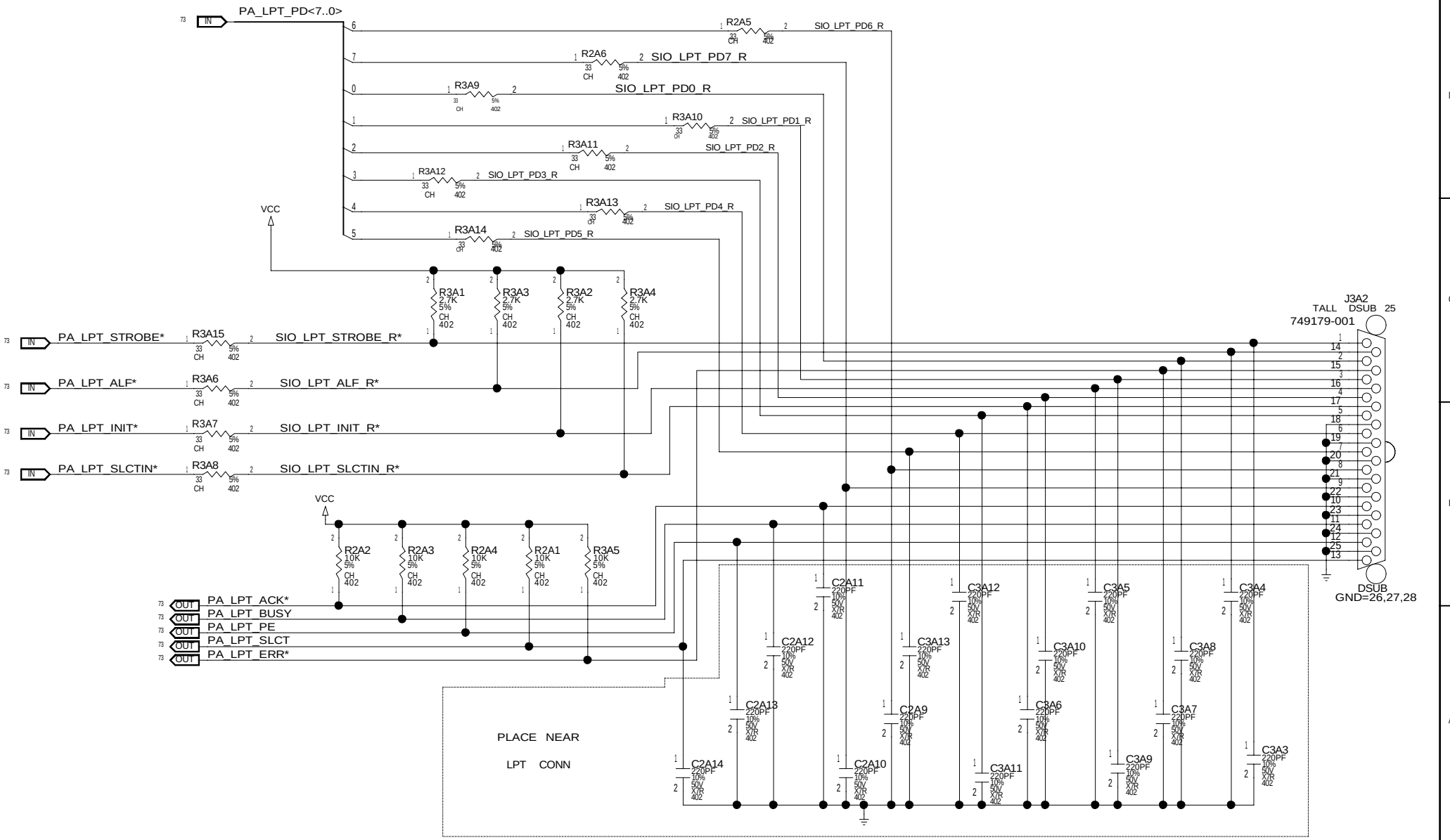
COMPONENTS ARE DFM29



[PAGE_TITLE=PS/2 MOUSE DOUBLE-STACKED]

DRAWING
D915PLWDL_FABA.SCH_1.76
Thu Apr 07 09:39:30 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	76	1.00



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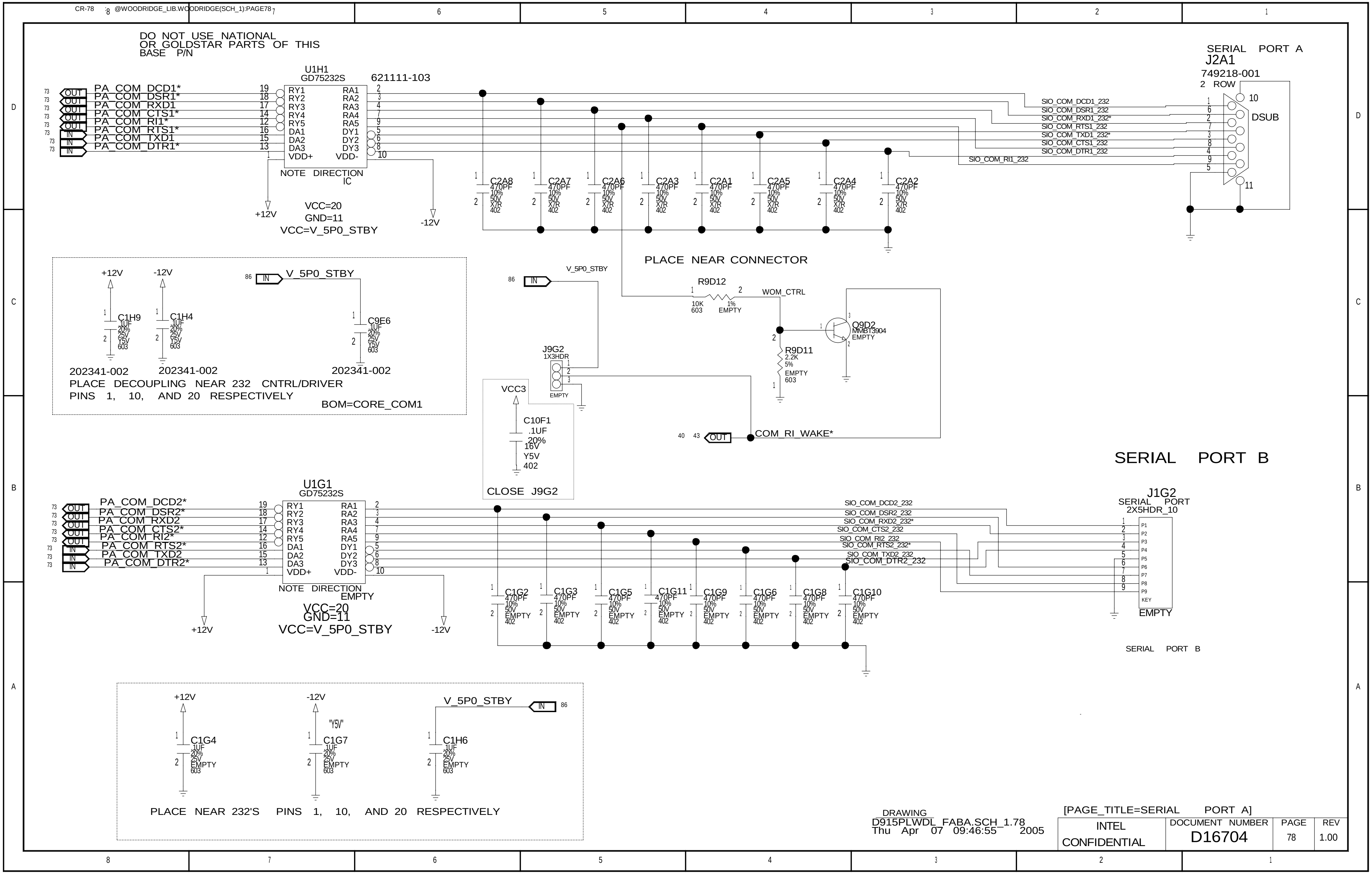
D915PLWDL_FABA.SCH_1.77
Thu Apr 07 09:39:34 2005

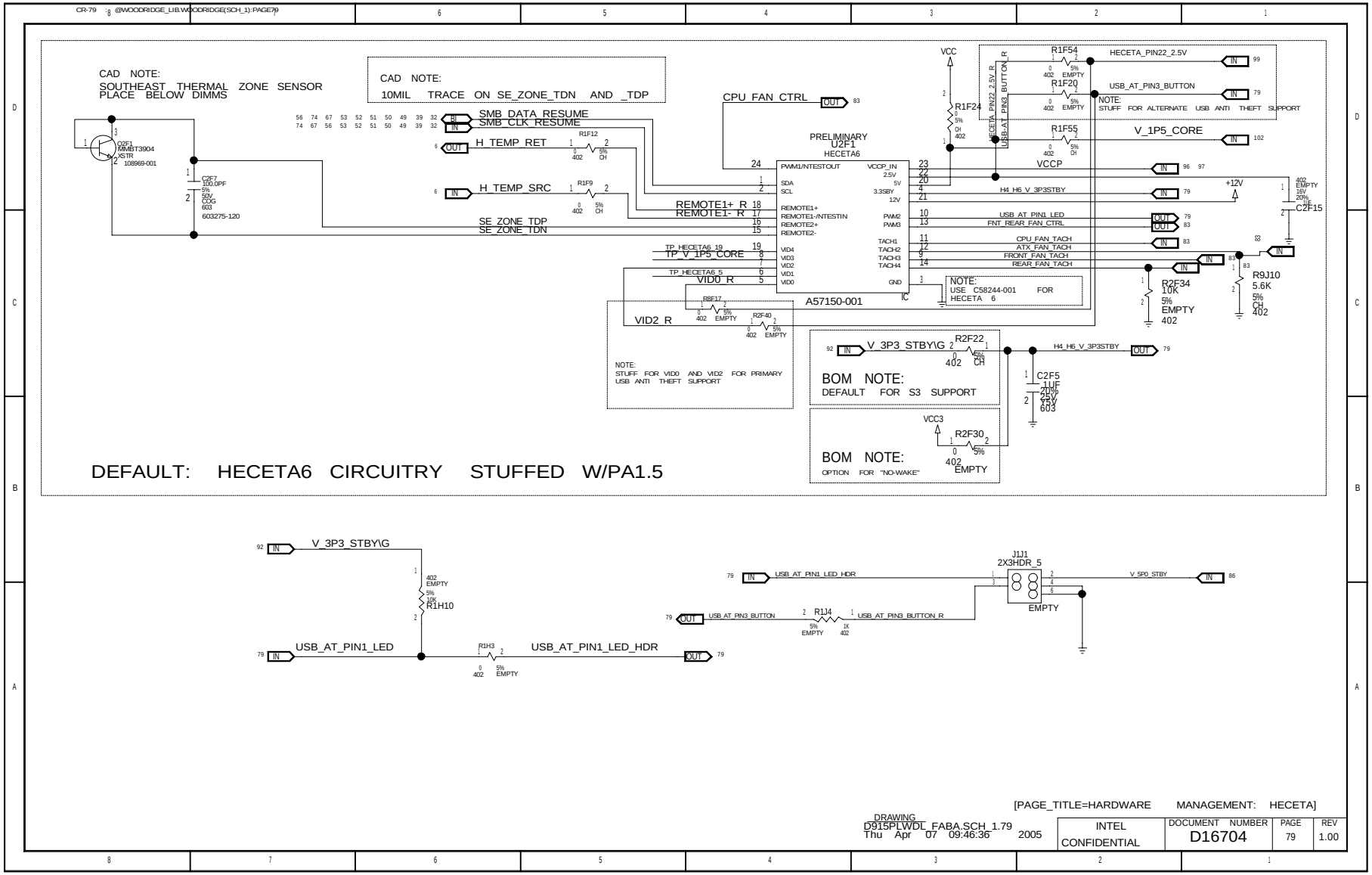
[PAGE_TITLE=LPT CONN]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	77	1.00



CR-78
@WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE78
DO NOT USE NATIONAL OR GOLDSTAR PARTS OF THIS BASE P/N
U1H1
GD75232S
621111-103
PA_COM_DCD1*
PA_COM_DSR1*
PA_COM_RXD1
PA_COM_CTS1*
PA_COM_RI1*
PA_COM_RTS1*
PA_COM_TXD1
PA_COM_DTR1*
NOTE DIRECTION IC
VCC=20
GND=11
VCC=V_5P0_STBY
+12V
-12V
C2A8 C2A7 C2A6 C2A3 C2A1 C2A5 C2A4 C2A2
470PF 10% 50V X7R 402
PLACE NEAR CONNECTOR
SERIAL PORT A
J2A1
749218-001
2 ROW
DSUB
SIO_COM_DCD1_232
SIO_COM_DSR1_232
SIO_COM_RXD1_232*
SIO_COM_RTS1_232
SIO_COM_TXD1_232*
SIO_COM_CTS1_232
SIO_COM_DTR1_232
SIO_COM_RI1_232
C1H9 C1H4 C9E6
.1UF 20% 25V Y5V 603
202341-002
PLACE DECOUPLING NEAR 232 CNTRL/DRIVER
PINS 1, 10, AND 20 RESPECTIVELY
BOM=CORE_COM1
V_5P0_STBY
R9D12
10K 603 1% EMPTY
WOM_CTRL
Q9D2
MMBT3904
EMPTY
R9D11
2.2K 5% EMPTY 603
J9G2
1X3HDR
EMPTY
VCC3
C10F1
.1UF 20% 16V Y5V 402
CLOSE J9G2
COM_RI_WAKE*
SERIAL PORT B
U1G1
GD75232S
PA_COM_DCD2*
PA_COM_DSR2*
PA_COM_RXD2
PA_COM_CTS2*
PA_COM_RI2*
PA_COM_RTS2*
PA_COM_TXD2
PA_COM_DTR2*
NOTE DIRECTION
EMPTY
VCC=20
GND=11
VCC=V_5P0_STBY
C1G2 C1G3 C1G5 C1G11 C1G9 C1G6 C1G8 C1G10
470PF 10% 50V EMPTY 402
J1G2
SERIAL PORT
2X5HDR_10
EMPTY
SIO_COM_DCD2_232
SIO_COM_DSR2_232
SIO_COM_RXD2_232*
SIO_COM_CTS2_232
SIO_COM_RI2_232
SIO_COM_RTS2_232*
SIO_COM_TXD2_232
SIO_COM_DTR2_232
SERIAL PORT B
C1G4 C1G7 C1H6
"Y5V"
.1UF 20% 25V EMPTY 603
PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY
DRAWING
D915PLWDL_FABA.SCH_1.78
Thu Apr 07 09:46:55 2005
[PAGE_TITLE=SERIAL PORT A]
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 78
REV 1.00

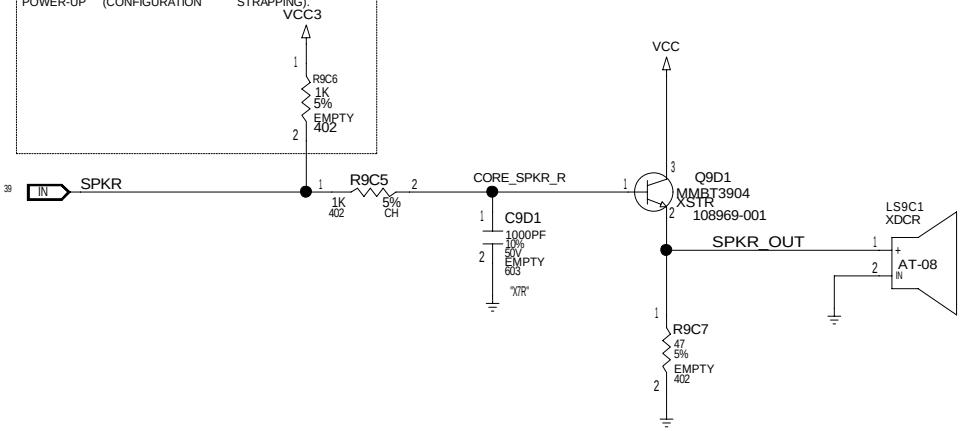
HECETA6 WILL BE EMPTY & "SATELLITE" HECETA WILL BE STUFFED IF PORT ANGELES 3.0 IS STUFFED

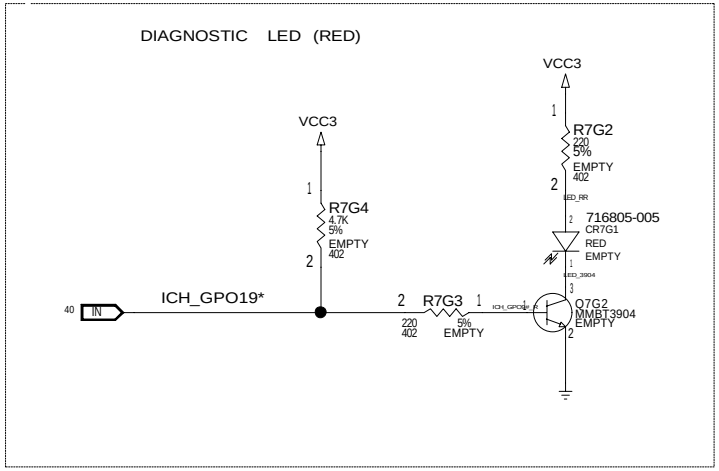


[PAGE_TITLE=HARDWARE MANAGEMENT: HECETA]

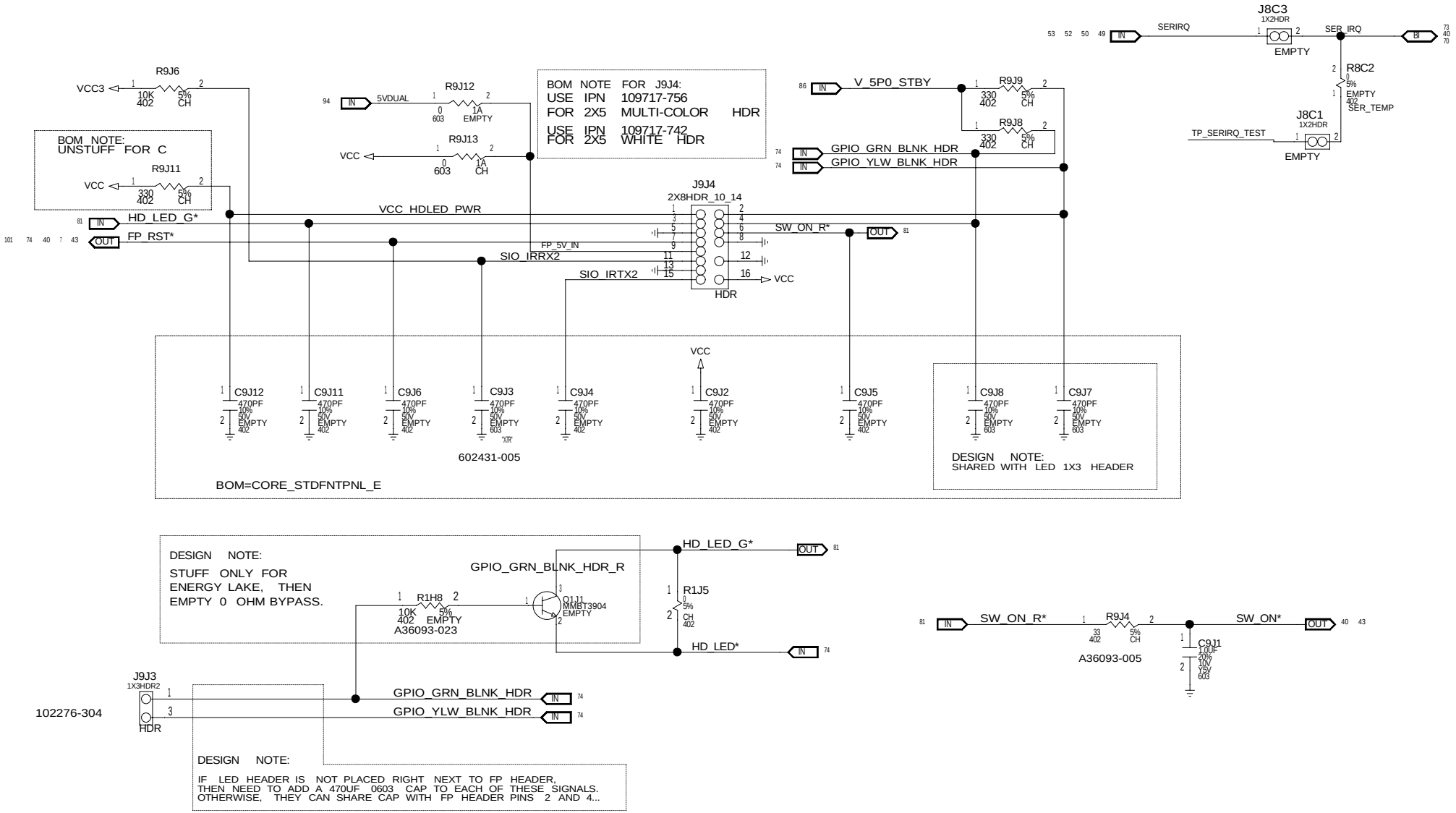
DRAWING				
D915PLWDL_FABA.SCH_1.79 Thu Apr 07 09:46:36 2005	INTEL CONFIDENTIAL	DOCUMENT NUMBER D16704	PAGE 79	REV 1.00

BOM NOTE:
STUFF TO DISABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).





[PAGE_TITLE=SPEAKER_DIAGNOSTIC_LED]



[PAGE_TITLE=STD_FRONT_PANEL_HDR]

DRAWING
D915PLWDL_FABA.SCH_1.81
Thu Apr 07 09:46:45 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	81	1.00

PB MOUNTING HOLES

J8A1 MTG_HOLE NC9 EMPTY

J7J1 MTG_HOLE NC9 EMPTY

J1G1 MTG_HOLE NC9 EMPTY

J1B1 MTG_HOLE NC9 EMPTY

J7G1 MTG_HOLE NC9 EMPTY

J1J3 MTG_HOLE NC9 EMPTY

J7A1 MTG_HOLE NC9 EMPTY

J9G1 MTG_HOLE NC9 EMPTY

A30094-001
LB6F1
LABEL
1500X150_TARGET

J11A2 MTG_HOLE NC9 EMPTY

J11J1 MTG_HOLE NC9 EMPTY

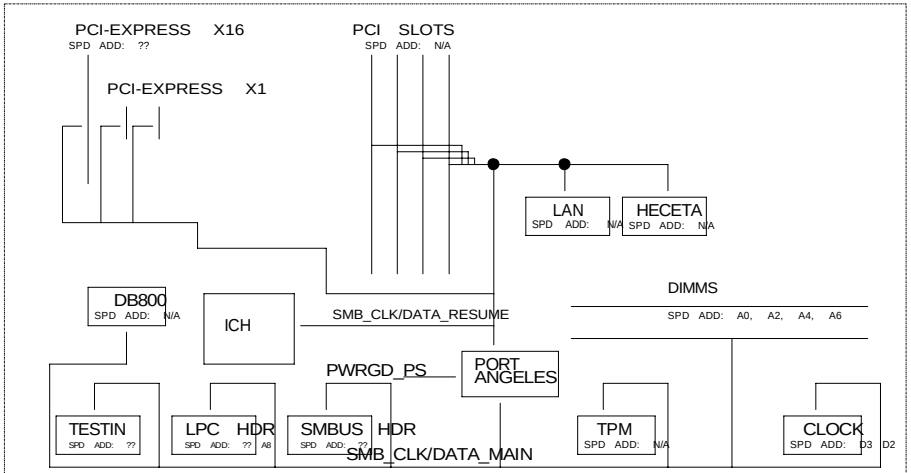
J11F1 MTG_HOLE NC9 EMPTY

200956-001; "CE" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED
628492-001; "FCC" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED (SECONDARY SIDE)
622954-001; "C-TICK" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED

LB4F2
LABEL
SILK
EMPTY
'KOREAN CERT' SILKSCREEN COVERED UNTIL CERTIFIED
MAKE EMPTY ON BOM

LB3F1
LABEL
A19177-001
1375X250_TARGET
CHANGE TO PROJECT ISN ON BOM (MOD-FILE CHANGE): CXXXXX-001

LB4F1
LABEL
'INTEL-BRANCH"
MAKE EMPTY ON BOM
A19202-001
2000X250_LOGO



SMB_CLK/DATA_MAIN

SECURITY (TPM)
PORT ANGELES
LPC BUS LAI HEADER
CLOCK
DIMMS (2 TIMES)

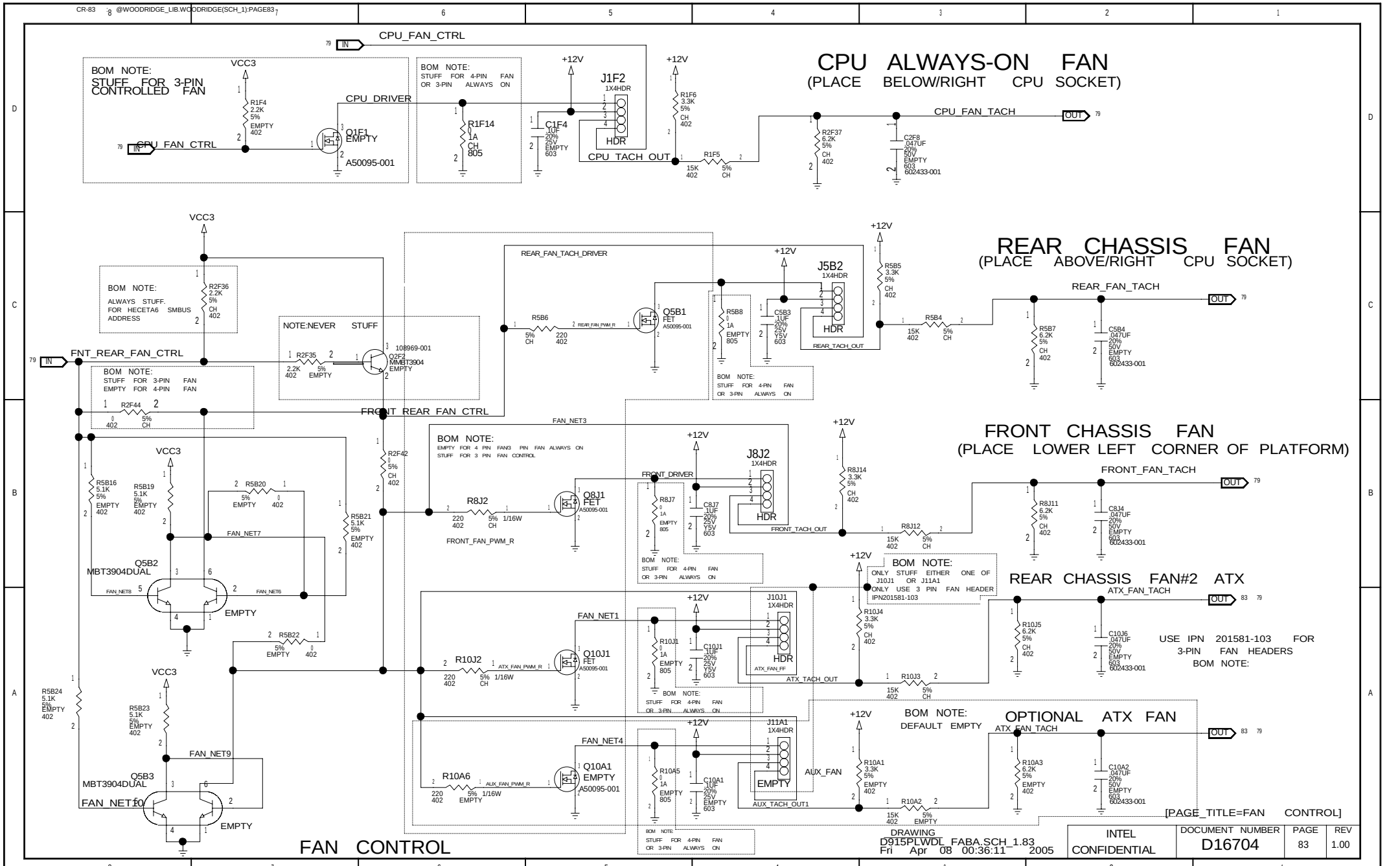
SMB_CLK/DATA_RESUME

PCI (4 TIMES)
LAN
HECETA
PORT ANGELES
ICH
PCI-EXPRESS X16
PCI-EXPRESS X1 (2 TIMES)

[PAGE_TITLE=MTG_HOLES/LABELS/SMBUS_MAP]

DRAWING
D915PLWDL_FABA.SCH_1.82
Thu Apr 07 17:53:41 2005

INTEL CONFIDENTIAL | DOCUMENT NUMBER D16704 | PAGE 82 | REV 1.00


CPU ALWAYS-ON FAN
(PLACE BELOW/RIGHT CPU SOCKET)
CPU_FAN_CTRL
CPU_DRIVER
CPU_TACH_OUT
CPU_FAN_TACH
REAR CHASSIS FAN
(PLACE ABOVE/RIGHT CPU SOCKET)
REAR_FAN_TACH_DRIVER
REAR_TACH_OUT
REAR_FAN_TACH
FNT_REAR_FAN_CTRL
FRONT_REAR_FAN_CTRL
FRONT CHASSIS FAN
(PLACE LOWER LEFT CORNER OF PLATFORM)
FRONT_DRIVER
FRONT_TACH_OUT
FRONT_FAN_TACH
FRONT_FAN_PWM_R
REAR CHASSIS FAN#2 ATX
ATX_FAN_TACH
ATX_TACH_OUT
ATX_FAN_PWM_R
USE IPN 201581-103 FOR 3-PIN FAN HEADERS
OPTIONAL ATX FAN
AUX_FAN
AUX_TACH_OUT1
AUX_FAN_PWM_R
FAN CONTROL
[PAGE_TITLE=FAN CONTROL]
D915PLWDL_FABA.SCH_1.83
Fri Apr 08 00:36:11 2005
INTEL CONFIDENTIAL
D16704
83
1.00

MODIFY THIS PAGE TO REFLECT APPROPRIATE SIGNALS

MCH

X.X (VCCP)

1.5 CORE

2.5 SM

2.5 STBY

ICH

3.3 (VCC3)

1.5 CORE

2.5 STBY

5.0 STBY

CK-410

3.3 (VCC3)

HEC6

3.3 STBY (VCC3 STBY)

5.0 (VCC)

12

X.X (VCCP)

1.5 (CORE)

SIO

3.3 (VCC3)

5.0 (VCC)

3.3 STBY (VCC3 STBY)

GLUECHIP

3.3 STBY (VCC3_STBY)

3.3 STBY (VCC3_STBY)

5.0 STBY (VCC STBY)

KINNERETH +

3.3 STBY (VCC3_STBY)

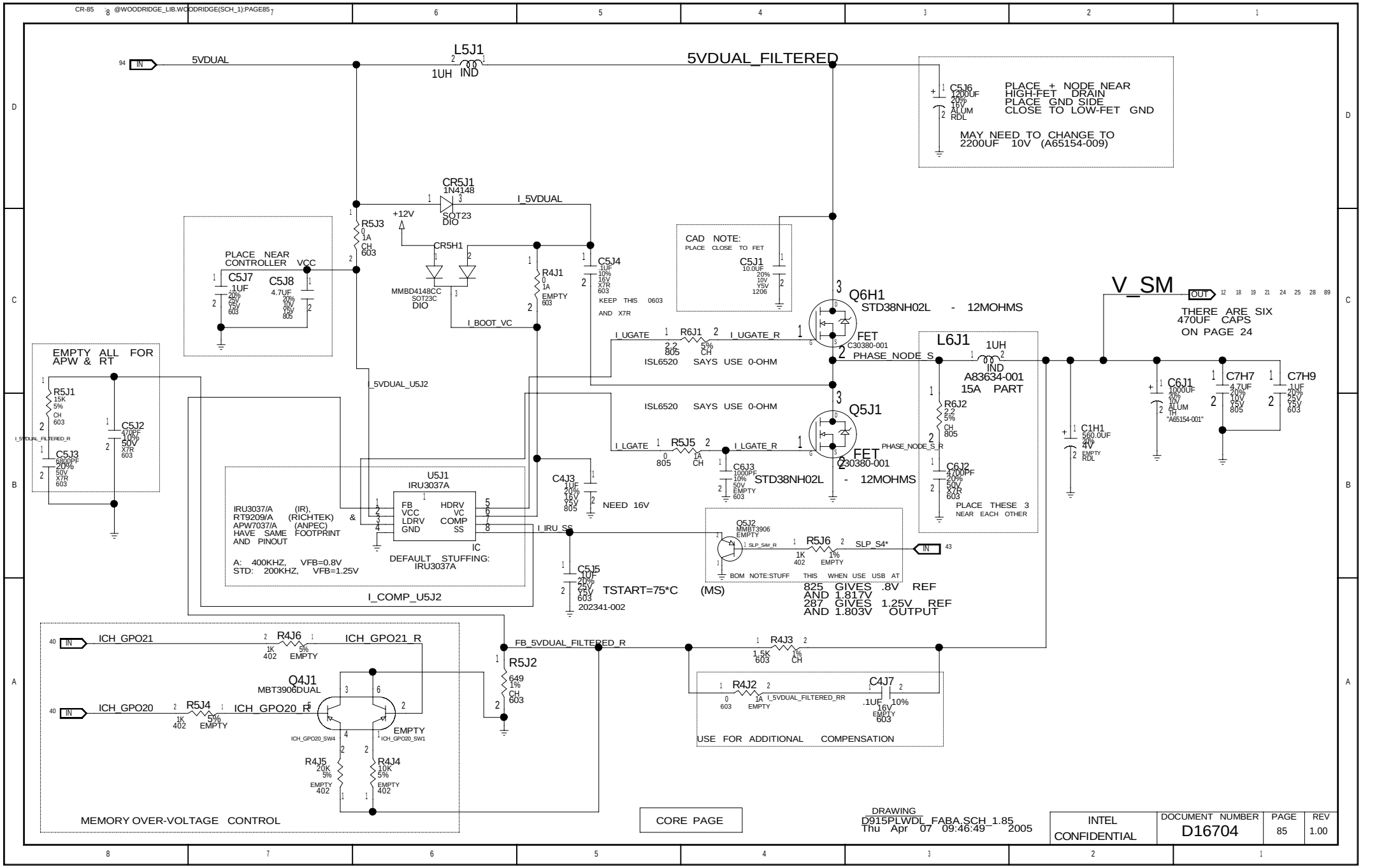
FWH

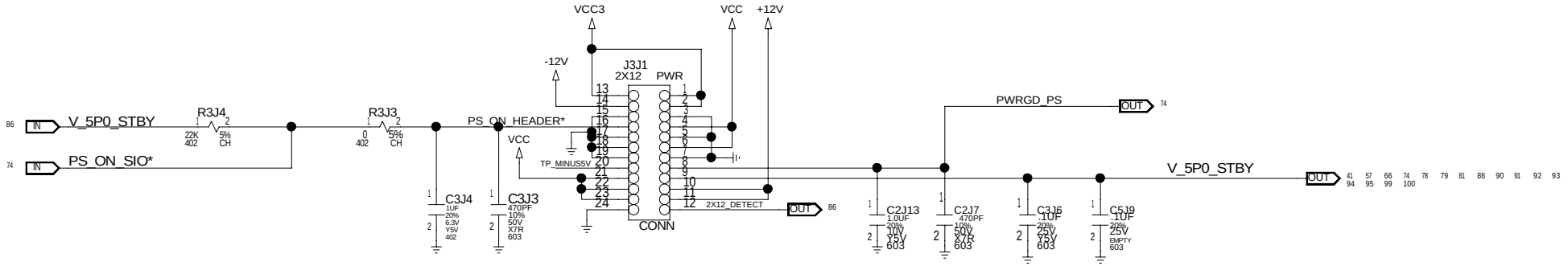
3.3 (VCC3)

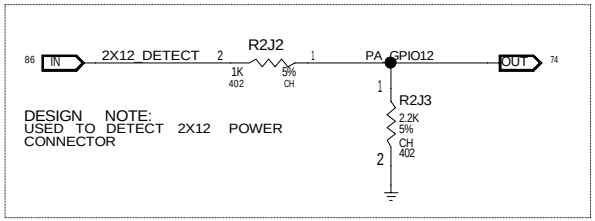
VREG_12V_FILTERED (+12V FILTERED FROM 12V POWER-SUPPLY)
VCCP (VTT, FOR NWD 1.29 - 1.45V)
V_1P25_MEMVTT (1.25V DERIVED FROM V_2.5)
V_2P5_SM (2.5V DERIVED FROM VCC)
VREG_USB_BP_LEFT (5.0 FROM VCC OR 5.0-STANDBY)
VREG_USB_BP_RIGHT (5.0 FROM VCC OR 5.0-STANDBY)
VREG_PS2 (5.0 FROM VCCC OR 5.0-STANDBY)
USB_FNT_PWR (5.0 FROM VCC OR 5.0-STANDBY)
USB_CNR_PWR (5.0 FROM VCC OR 5.0-STANDBY)
V_3P3_PCI_VAUX (3.3V OR 3.3-STANDBY SOURCE)
V_3P3_STBY (3.3V DERIVED FROM 5.0-STANDBY)
V_5P0_STBY (5.0V FROM POWER-SUPPLY)
V_BAT_VREG_R_CR (3.0V FROM THE BATTERY)
V_3P0_BAT_VREG (~3.0V FROM THE BATTERY THROUGH A DIODE)
+12V (PLUS 12V FROM POWER-SUPPLY)
-12V (MINUS 12V FROM POWER-SUPPLY)
VCC3 (3.3V FROM POWER-SUPPLY)
VCC (5.0V FROM POWER-SUPPLY)

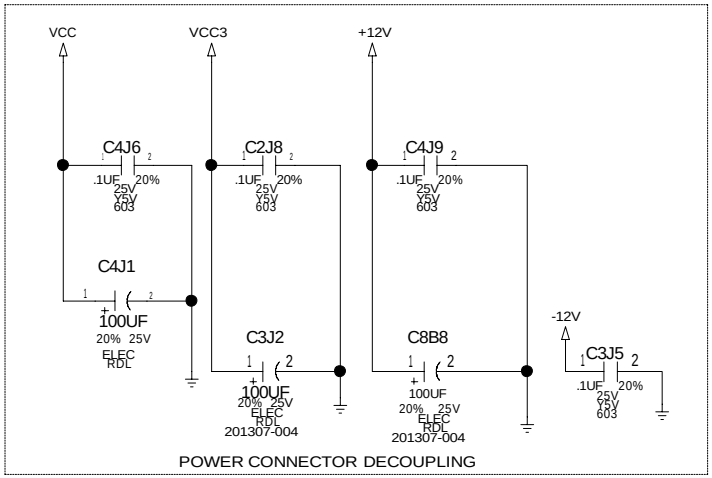
V_1P5_CORE (NOT CONNECTED)
V_1P25_MEMVTT_B (NOT CONNECTED)
V_1P3_NOMINAL (NOT CONNECTED)
V_1P5_AGP (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)
V_12VREG (NOT CONNECTED)
V_AGP_VDDQ (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)

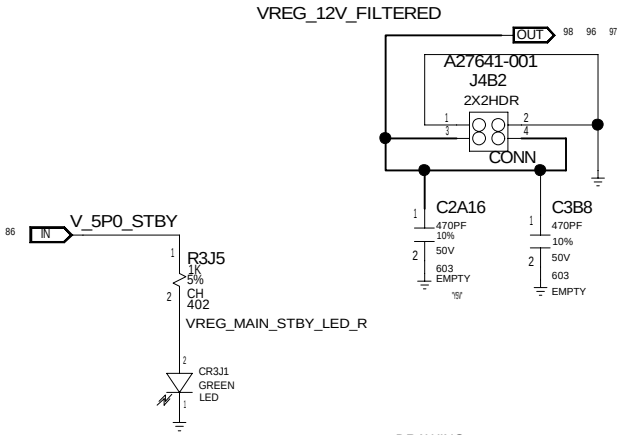
[PAGE_TITLE=VREG: VOLTAGE DISTRIBUTION]


CR-85 :8 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE85 :7
5VDUAL
L5J1
1UH IND
5VDUAL_FILTERED
C5J6 1200UF 20% 16V ALUM RDL
PLACE + NODE NEAR HIGH-FET DRAIN
PLACE GND SIDE CLOSE TO LOW-FET GND
MAY NEED TO CHANGE TO 2200UF 10V (A65154-009)
CR5J1 1N4148 SOT23 DIO
I_5VDUAL
+12V
R5J3 0 1A CH 603
CR5H1
MMBD4148CC SOT23C DIO
R4J1 0 1A EMPTY 603
C5J4 1UF 10% 16V X7R 603
KEEP THIS 0603 AND X7R
I_BOOT_VC
PLACE NEAR CONTROLLER VCC
C5J7 1UF 20% 25V Y5V 603
C5J8 4.7UF 20% 10V Y5V 805
CAD NOTE: PLACE CLOSE TO FET
C5J1 10.0UF 20% 10V Y5V 1206
Q6H1 STD38NH02L - 12MOHMS
FET C30380-001
PHASE_NODE_S
I_UGATE
R6J1 2.2 5% 805 CH
I_UGATE_R
ISL6520 SAYS USE 0-OHM
V_SM
OUT
THERE ARE SIX 470UF CAPS ON PAGE 24
L6J1 1UH IND A83634-001 15A PART
R6J2 2.2 5% CH 805
C6J2 4700PF 20% 50V X7R 603
PLACE THESE 3 NEAR EACH OTHER
C6J1 1000UF 20% 10V ALUM TH "A65154-001"
C7H7 4.7UF 20% 10V Y5V 805
C7H9 1UF 20% 25V Y5V 603
C1H1 560.0UF 20% 4V EMPTY RDL
EMPTY ALL FOR APW & RT
R5J1 15K 5% CH 603
C5J2 470PF 10% 50V X7R 603
C5J3 6800PF 20% 50V X7R 603
I_5VDUAL_FILTERED_R
I_5VDUAL_U5J2
ISL6520 SAYS USE 0-OHM
Q5J1
FET C30380-001
STD38NH02L - 12MOHMS
I_LGATE
R5J5 0 805 1A CH
I_LGATE_R
PHASE_NODE_S_R
C6J3 1000PF 10% 50V EMPTY 603
U5J1 IRU3037A
FB VCC LDRV GND HDRV VC COMP SS
IC
IRU3037A (IR), RT9209/A (RICHTEK) & APW7037A (ANPEC) HAVE SAME FOOTPRINT AND PINOUT
A: 400KHZ, VFB=0.8V
STD: 200KHZ, VFB=1.25V
DEFAULT STUFFING: IRU3037A
C4J3 1UF 20% 16V Y5V 805
NEED 16V
I_IRU_SS
Q5J2 MMBT3906 EMPTY
R5J6 1K 1% 402 EMPTY
SLP_S4*
BOM NOTE:STUFF THIS WHEN USE USB AT
C5J5 .1UF 20% 25V 603 202341-002
TSTART=75*C (MS)
825 GIVES .8V REF AND 1.817V
287 GIVES 1.25V REF AND 1.803V OUTPUT
I_COMP_U5J2
ICH_GPO21
R4J6 1K 5% 402 EMPTY
ICH_GPO21_R
Q4J1 MBT3906DUAL
ICH_GPO20
R5J4 1K 5% 402 EMPTY
ICH_GPO20_R
ICH_GPO20_SW4
ICH_GPO20_SW1
EMPTY
R4J5 20K 5% EMPTY 402
R4J4 10K 5% EMPTY 402
FB_5VDUAL_FILTERED_R
R5J2 649 1% CH 603
R4J3 1.5K 1% 603 CH
R4J2 0 603 1A EMPTY
I_5VDUAL_FILTERED_RR
C4J7 .1UF 10% 16V EMPTY 603
USE FOR ADDITIONAL COMPENSATION
MEMORY OVER-VOLTAGE CONTROL
CORE PAGE
DRAWING D915PLWDL_FABA.SCH 1.85 Thu Apr 07 09:46:49 2005
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 85
REV 1.00







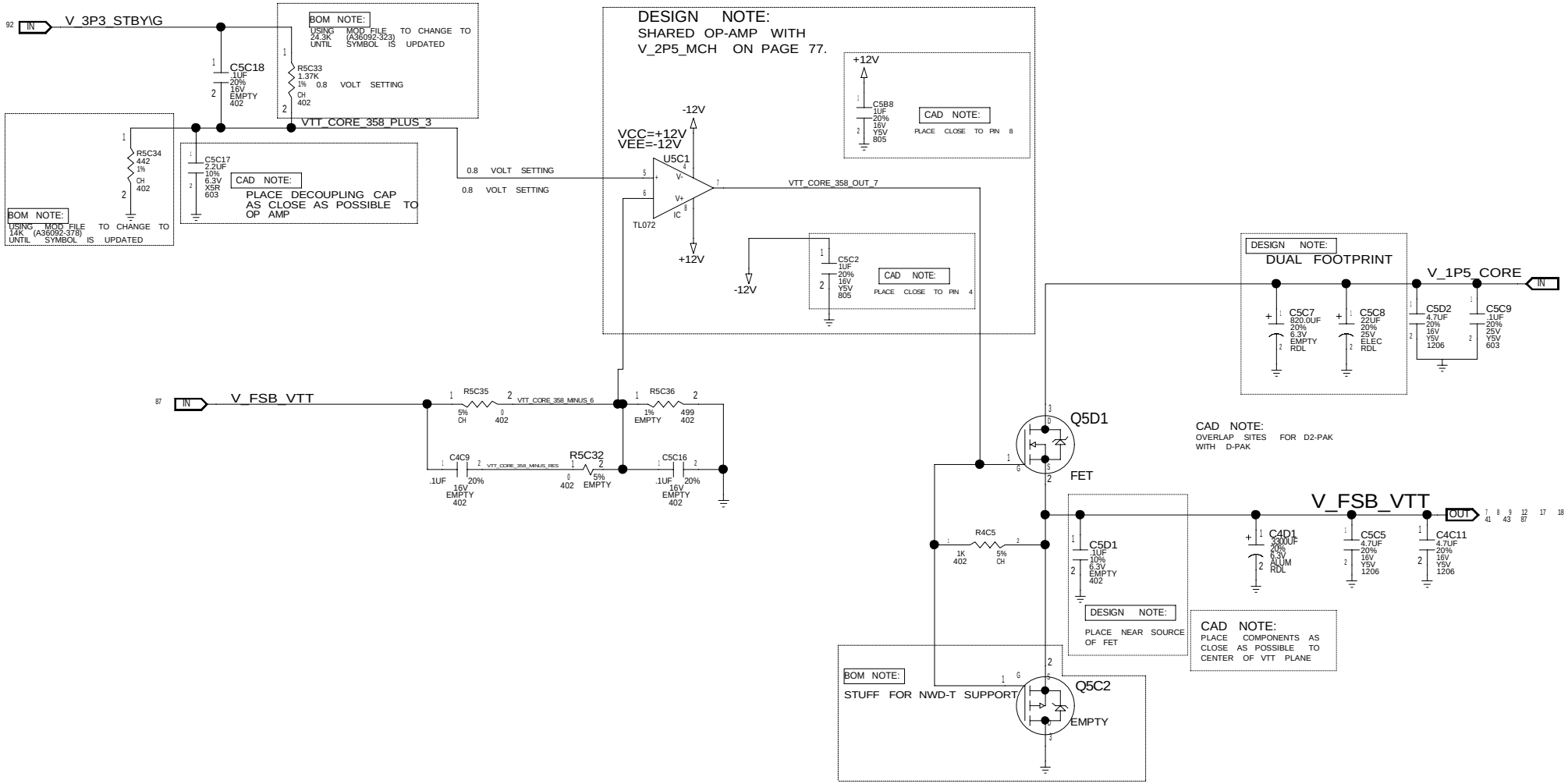


[PAGE_TITLE=STANDARD POWER CONNECTOR]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.86
Thu Apr 07 09:54:50 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	86	1.00

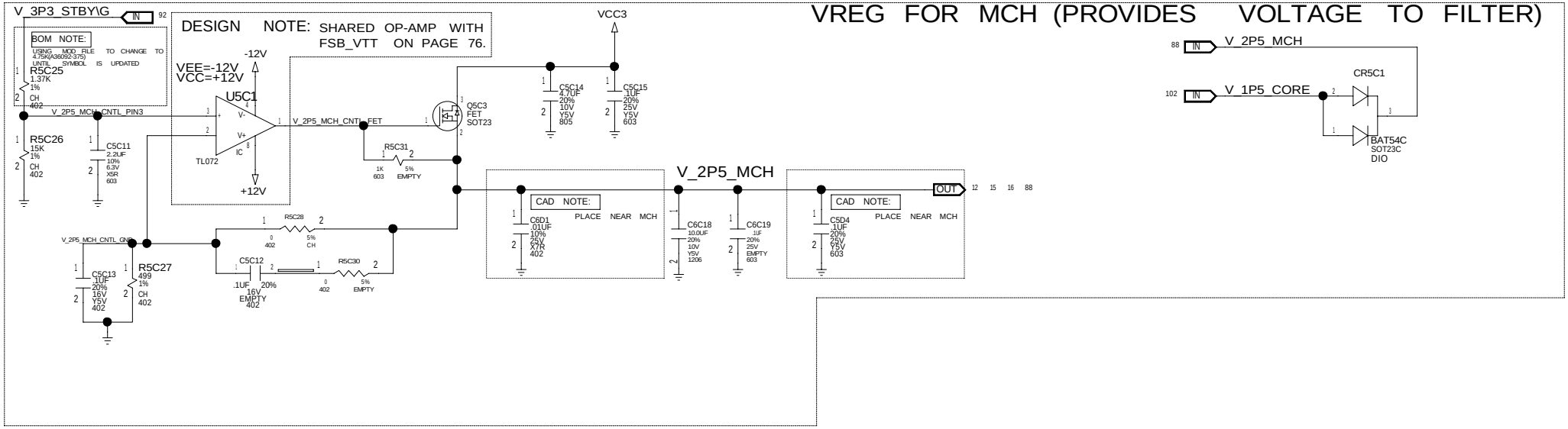


[PAGE_TITLE=VREG: FSB VTT]

DRAWING
D915PLWDL_FABA.SCH_1.87
Thu Apr 07 00:17:11 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	87	1.00

VREG FOR MCH (PROVIDES VOLTAGE TO FILTER)



[PAGE_TITLE=VREG 2P5 MCH

DRAWING
D915PLWDL_FABA.SCH_1.88
Thu Apr 07 00:17:44 2005

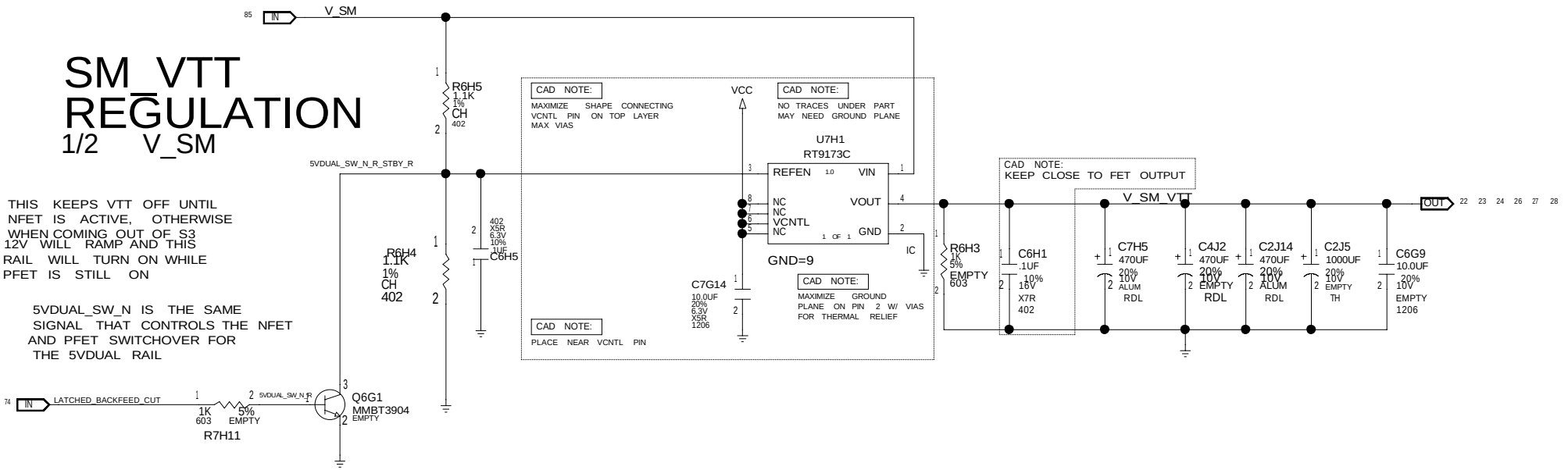
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	88	1.00

SM_VTT REGULATION

1/2 V_SM

THIS KEEPS VTT OFF UNTIL NFET IS ACTIVE, OTHERWISE WHEN COMING OUT OF S3 12V WILL RAMP AND THIS RAIL WILL TURN ON WHILE PFET IS STILL ON

5VDUAL_SW_N IS THE SAME SIGNAL THAT CONTROLS THE NFET AND PFET SWITCHOVER FOR THE 5VDUAL RAIL



CORE PAGE

DRAWING D915PLWDL_FABA.SCH_1.89 Thu Apr 07 00:17:16 2005

[PAGE_TITLE=VREG_SM_VTT]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	89	1.00

BATTERY CR7J1

92 IN V_3P3_STBY\G 2 3 V_3P0_BAT_VREG OUT 39 41 43

1 R7J1 2 1K 402 5% CH I_VREG_VBAT_R 1 BAT54C SOT23C DIO

1 C9H4 2 1.0UF 20% 10V Y5V 603

CAD NOTE: PLACE NEAR ICH

XBT7J1 VREG_VBAT_R 1 2 2PCOIN A05835-001

THROUGH-HOLE FLAT BATTERY

CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

90 IN VREG_USB_NCH_PCI 1 G Q8C3 3 D S 2 EMPTY

VCC3

90 IN VREG_USB_PCH_PCI 1 G Q8C2 3 D S 2 EMPTY

92 IN V_3P3_STBY\G

92 IN V_3P3_STBY\G 1 RP9C2 0 5% .063W IC 2 RP9C2 0 5% .063W IC 3 RP9C2 0 5% .063W IC 4 RP9C2 0 5% .063W IC 8 7 6 5

CAD NOTE: PLACE AT PCI SLOTS

V_3P3_PCIVAUX OUT 90 56 32 57 49 58 50 59 51 67 52 53

1 C7C3 2 100UF 20% 25V ELEC RDL

1 C8C2 2 .1UF 20% 25V EMPTY 603

1 C7C2 2 .1UF 20% 25V Y5V 603

1 C9C1 2 .1UF 20% 25V EMPTY 603

1 C8C1 2 .1UF 20% 25V EMPTY 603

[PAGE_TITLE=PCI VAUX]

86 IN V_5P0_STBY

+12V

RP9J2 2.7K 5% .063W IC SM 3 4 5 6

74 IN LATCHED_BACKFEED_CUT RP9J1 3 6 2.7K SM 5% .063W IC VREG_BFEED_R_NU

Q9J1 MBT3904DUAL 3 6 5 2 4 1 XSTR

RP9J1 5 4 2.7K SM 5% .063W IC VREG_BFEED_RR_NU

RP9J1 1 8 2.7K SM 5% .063W IC VREG_BFEED_R1_NU

RP9J1 2 7 2.7K SM 5% .063W IC VREG_BFEED_R2_NU

CONTROL SIGNAL FOR 4-DIMM VREG CONTROLLER

VREG_USB_NCH_L OUT 90

VREG_USB_PCH_L OUT 90

90 IN VREG_USB_NCH_L 1 R9J7 2 0 402 5% CH VREG_USB_NCH OUT 90 94

90 IN VREG_USB_PCH_L 1 R9J5 2 0 402 5% CH VREG_USB_PCH OUT 90 94

A

NOTES:

USB/PS2WAKE	A	B
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF

90 IN VREG_USB_NCH_PCI 1 R9C1 2 0 402 5% EMPTY VREG_USB_NCH OUT 90 94

90 IN VREG_USB_PCH_PCI 1 R9C2 2 0 402 5% EMPTY VREG_USB_PCH OUT 90 94

B

92 IN V_3P3_STBY\G 1 R9C9 2 0 2010 2A EMPTY V_3P3_PCIVAUX OUT 53 90 50 58 56 32 51 59 57 49 52 67

DESIGN NOTE: COST REDUCTON EXPERIMENT

RP9B1 TP_VREG_LINEAR_RP_2 1 2 8.2K SM 5% .063W IC TP_VREG_LINEAR_RP_7

RP9B1 TP_VREG_LINEAR_RP_8 6 3 8.2K SM 5% .063W IC TP_VREG_LINEAR_RP_1

SPARE SECTIONS

RP9J2 TP_VREG_LINEAR2_RP_7 1 2 2.7K SM 5% .063W IC TP_VREG_LINEAR2_RP_2

RP9J2 TP_VREG_LINEAR2_RP_3 .063W 5% IC 8 2.7K SM TP_VREG_LINEAR2_RP_6

SPARE SECTIONS

86 IN V_5P0_STBY

+12V

RP9B1 8.2K 5% .063W IC SM 4 1 5 8 8.2K SM IC .063W 5% RP9B1

VREG_USB_NCH_PCI OUT 90

VREG_USB_PCH_PCI OUT 90

74 IN BACKFEED_CUT .063W RP8B3 2 7 5% IC 2.7K SM VREG_BFEED_R

Q8C1 MBT3904DUAL 3 6 5 2 4 1 EMPTY

RP8B3 8 1 2.7K SM 5% .063W IC VREG_BFEED_RR

RP8B3 4 5 2.7K SM 5% .063W IC VREG_BFEED_R1

Q3J1 MMBT3904 EMPTY 1 3 2

1-WATT IN 73

R8C3 2 1 5% EMPTY 0 402

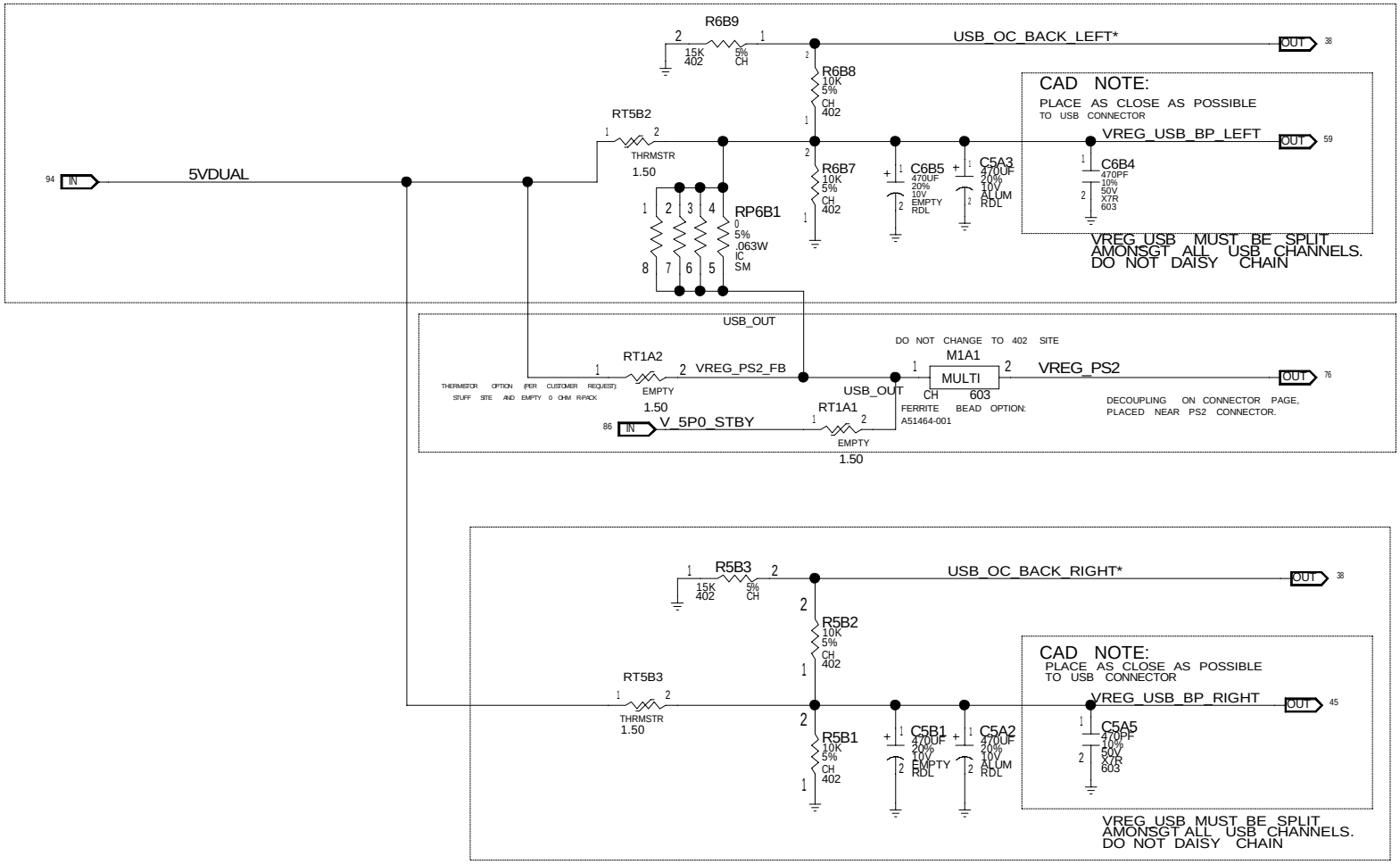
LATCHED_BACKFEED_CUT IN 74

RP8B3 3 6 .063W 5% IC 2.7K SM

CORE PAGE

DRAWING D915PLWDL_FABA.SCH_1.90 Thu Apr 07 00:17:21 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	90	1.00



[PAGE_TITLE=USB_BP_RIGHT/LEFT PS2]

DRAWING
D915PLWDL_FABA.SCH_1.91
Thu Apr 07 00:17:31 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	91	1.00

CAD NOTE:
OVERLAPPING SITE.
DESIGN NOTE:
DUAL-SITE INCLUDED TO FORCE FOOTPRINT KEEPOUT:
UN-STUFFED, BUT MAY BE USED IN PRODUCTION DESIGNS.

ADJ
U10E2
MC33269
IN
OUT
ADJ
SM

U10E1
EZ1086
IN
OUT
ADJ/GND
3.3V
EMPTY

86 IN V_5P0_STBY
C9D6
1.0UF
20%
10V
Y5V
603

R10E2
274
1%
CH
402
NOTE:
EMPTY FOR EZ1086
STUFF FOR MC33269

I_ADJUST_R

C9E5
1UF
20%
25V
EMPTY
603

R10E1
453
1%
CH
402
NOTE:
STUFF 45.3 OHM FOR MC33269
STUFF 0OHM FOR EZ1086

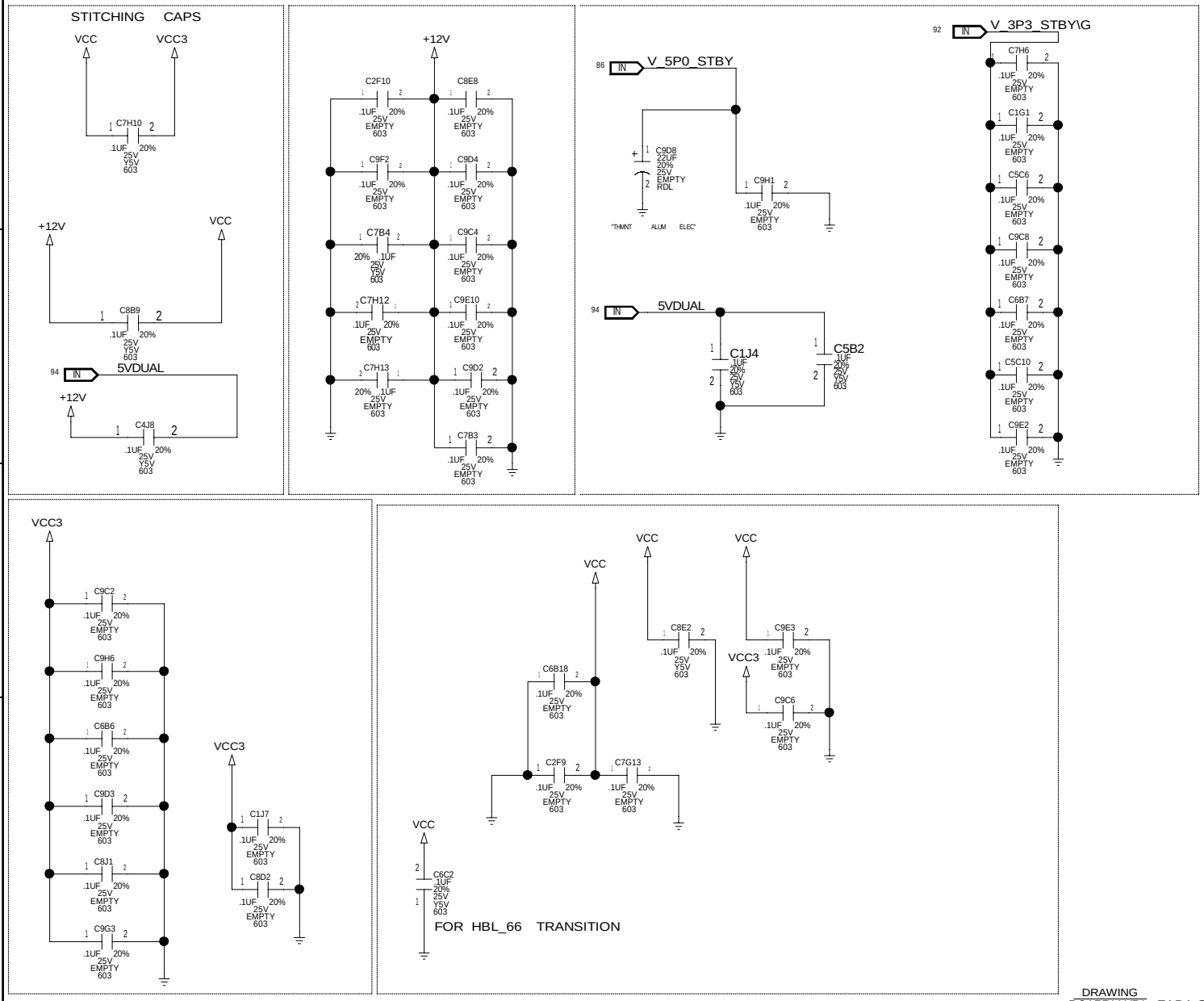
V_3P3_STBY\G
OUT 29 79 38 87 39 88 40 90 41 93 43 95 55 99 56 73 74
C9E1
220UF
20%
25V
ELEC
RDL

[PAGE_TITLE=3.3V STANDBY]

CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.92
Thu Apr 07 00:17:49 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	92	1.00



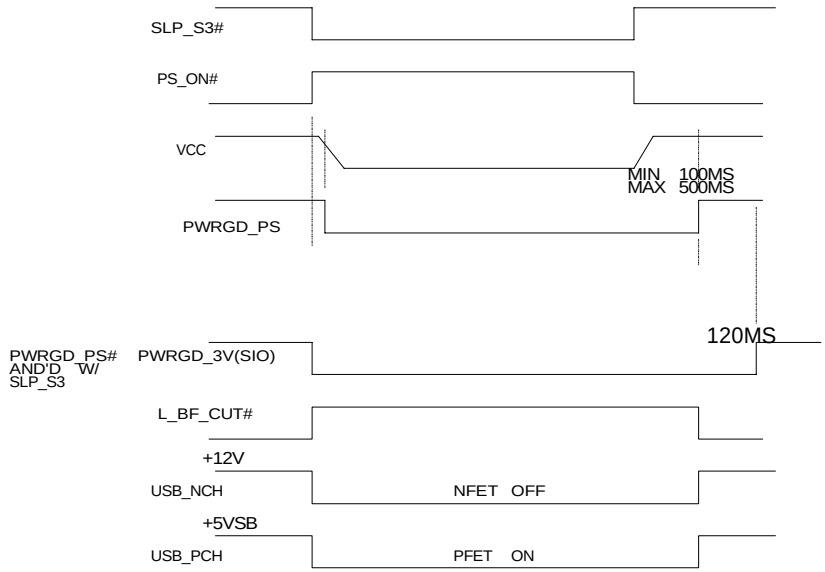
CORE PAGE

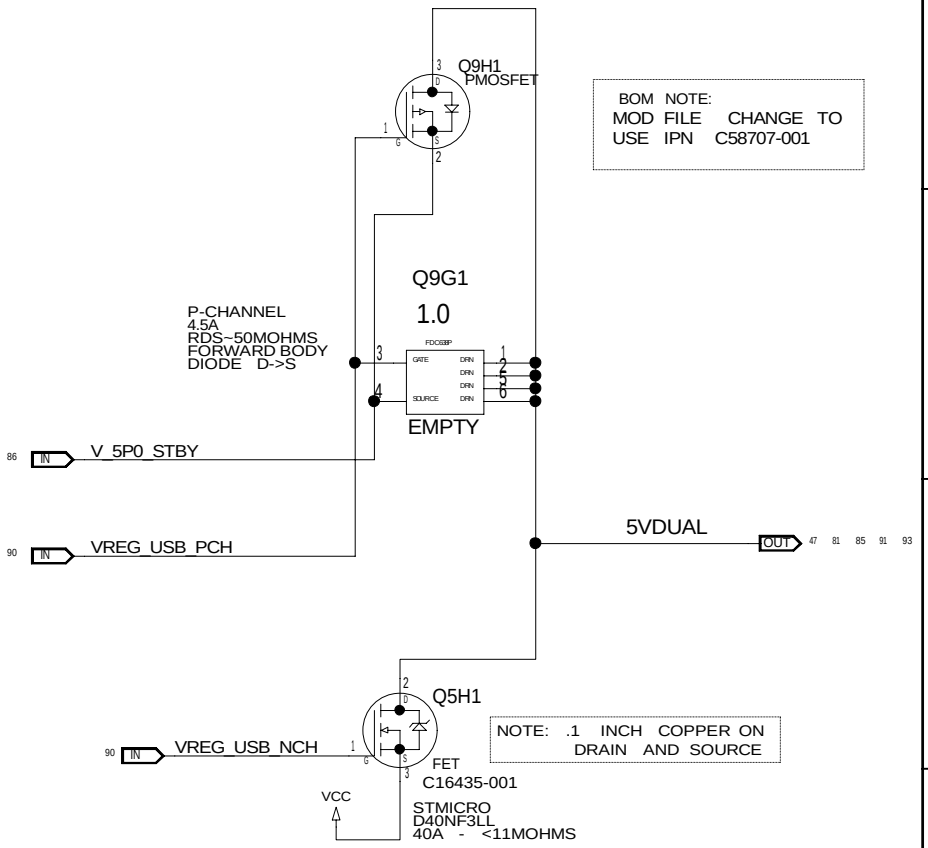
ROOM=DCPL_BULK
BOM=VREG_DCPL_BULK

DRAWING
D915PLWDL_FABA.SCH_1.93
Thu Apr 07 00:17:35 2005

[PAGE_TITLE=VREG_DCPL_BULK]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	93	1.00



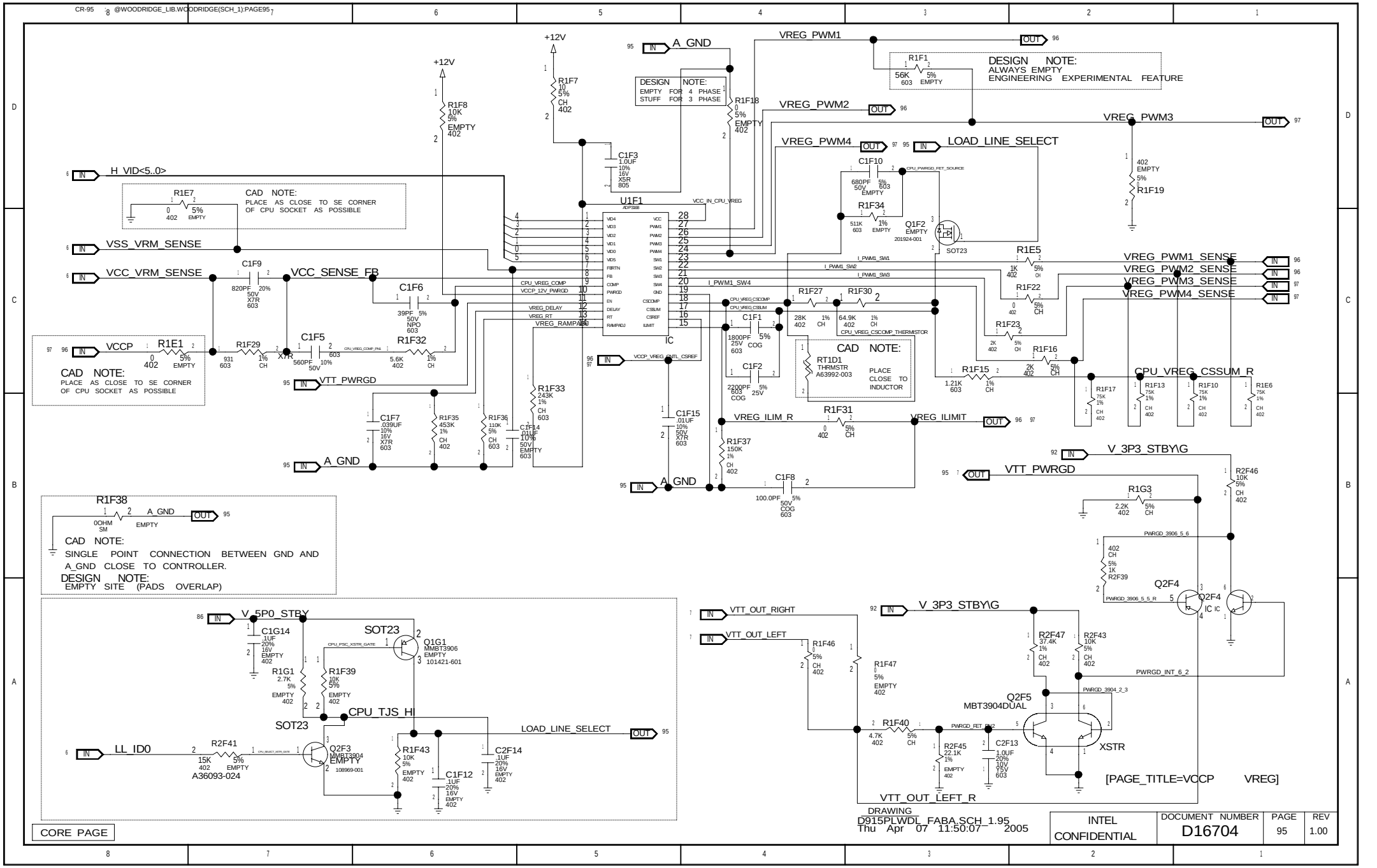


CORE PAGE

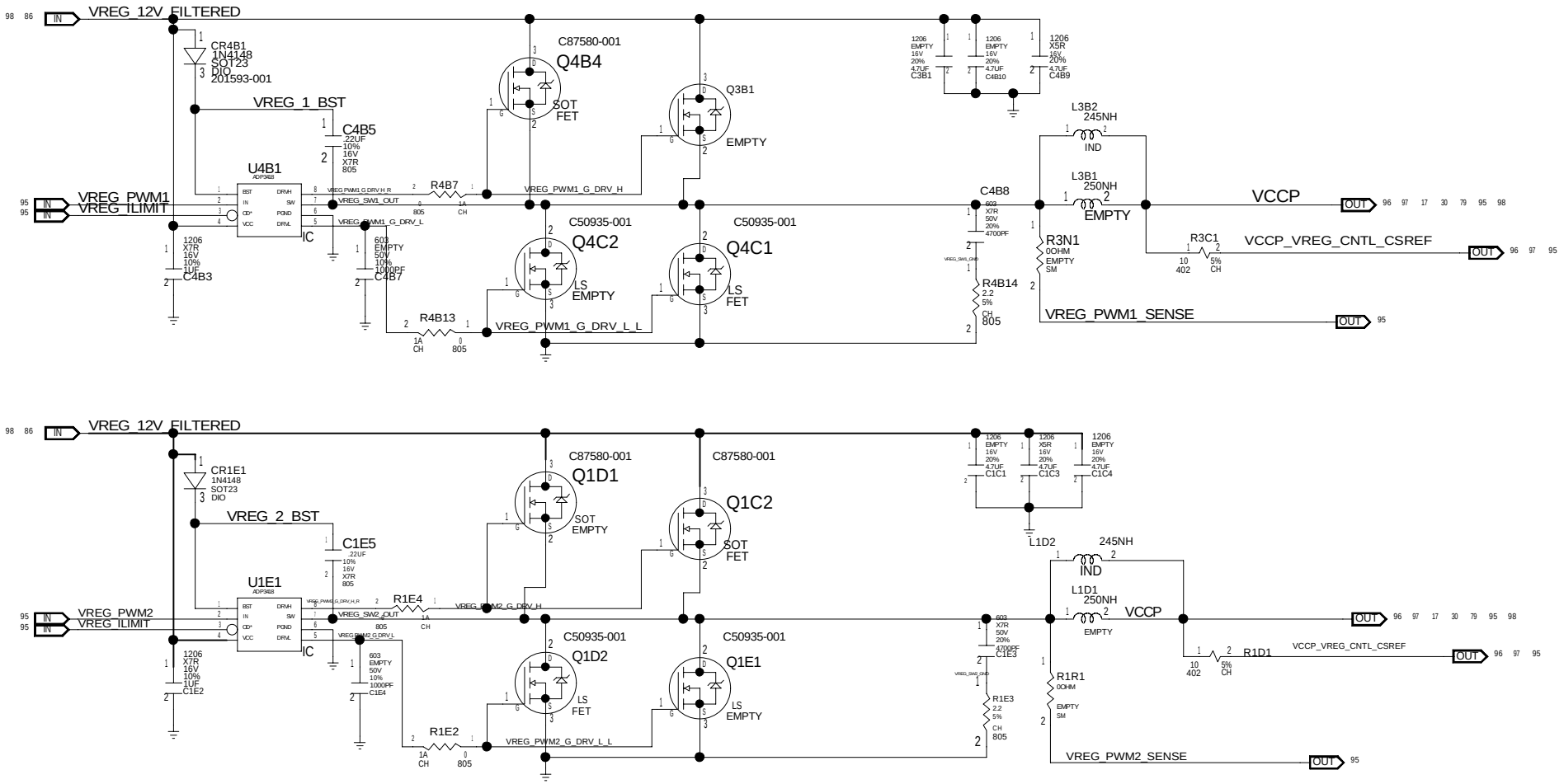
[PAGE_TITLE=5VDUAL/USB_BP_MID]

DRAWING
D915PLWDL_FABA.SCH_1.94
Thu Apr 07 11:31:29 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	94	1.00


CR-95 :8 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE95
+12V
A_GND
VREG_PWM1
VREG_PWM2
VREG_PWM3
VREG_PWM4
LOAD_LINE_SELECT
H_VID<5..0>
VSS_VRM_SENSE
VCC_VRM_SENSE
VCC_SENSE_FB
VCCP
VTT_PWRGD
VREG_ILIMIT
VREG_PWM1_SENSE
VREG_PWM2_SENSE
VREG_PWM3_SENSE
VREG_PWM4_SENSE
CPU_VREG_CSSUM_R
V_3P3_STBY\G
V_5P0_STBY
LL_ID0
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_OUT_LEFT_R
CAD NOTE:
PLACE AS CLOSE TO SE CORNER OF CPU SOCKET AS POSSIBLE
DESIGN NOTE:
ALWAYS EMPTY
ENGINEERING EXPERIMENTAL FEATURE
DESIGN NOTE:
EMPTY FOR 4 PHASE
STUFF FOR 3 PHASE
CAD NOTE:
SINGLE POINT CONNECTION BETWEEN GND AND A_GND CLOSE TO CONTROLLER.
DESIGN NOTE:
EMPTY SITE (PADS OVERLAP)
CAD NOTE:
PLACE CLOSE TO INDUCTOR
RT1D1
THRMSTR
A63992-003
U1F1
ADP3188
IC
Q1F2
SOT23
Q1G1
MMBT3906
Q2F3
MMBT3904
Q2F4
Q2F5
MBT3904DUAL
XSTR
CPU_TJS_HI
[PAGE_TITLE=VCCP VREG]
DRAWING
D915PLWDL_FABA.SCH_1.95
Thu Apr 07 11:50:07 2005
INTEL CONFIDENTIAL
DOCUMENT NUMBER D16704
PAGE 95
REV 1.00
CORE PAGE

BOM NOTE: Q1D1 Q4B4
PRIMARY C99215-001
SECONDARY C87580-001



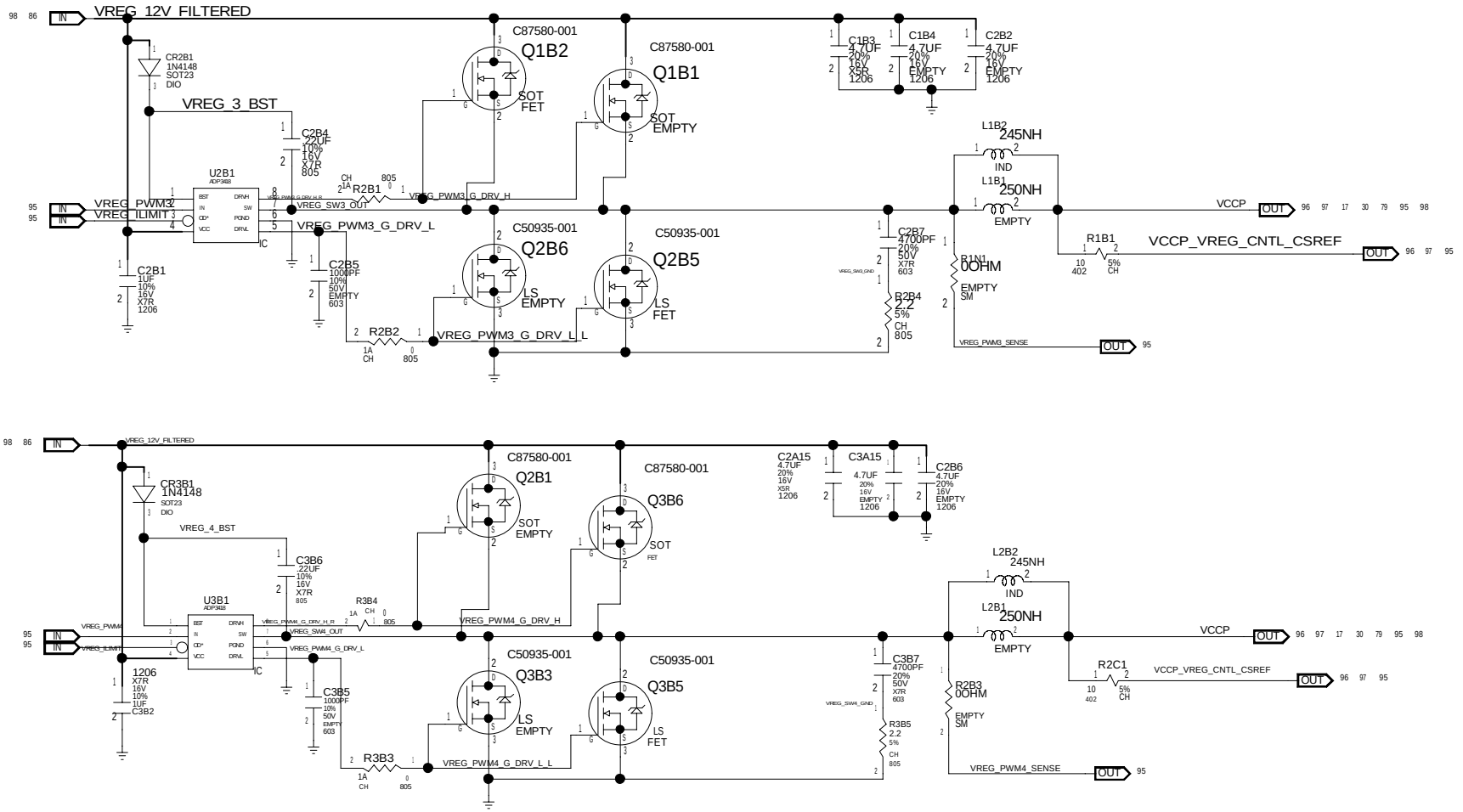
CORE PAGE

DRAWING
D915PLWDL_FABA.SCH 1.96
Thu Apr 07 20:49:18 2005

[PAGE_TITLE=VCCP VREG]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	96	1.00

BOM NOTES: Q2B1 Q1B2
PRIMARY C99215-001
ALTERNATE C87580-001



[PAGE_TITLE=VCCP VREG]

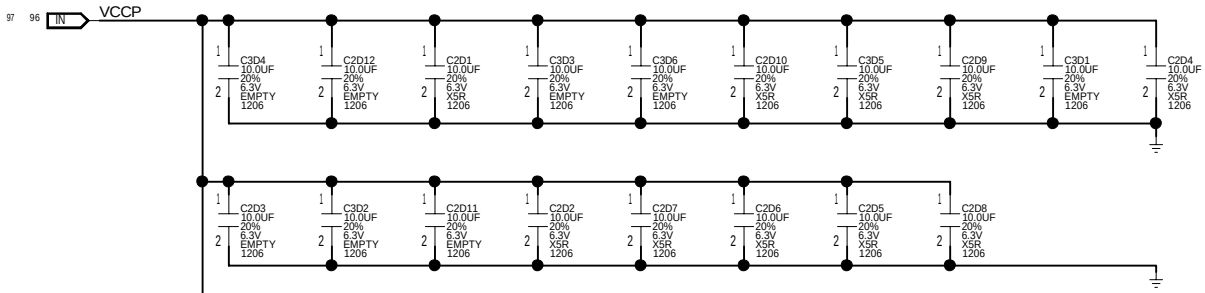
CORE PAGE

DRAWING
D915PLWDL_FABA.SCH_1.97
Thu Apr 07 20:48:33 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	97	1.00

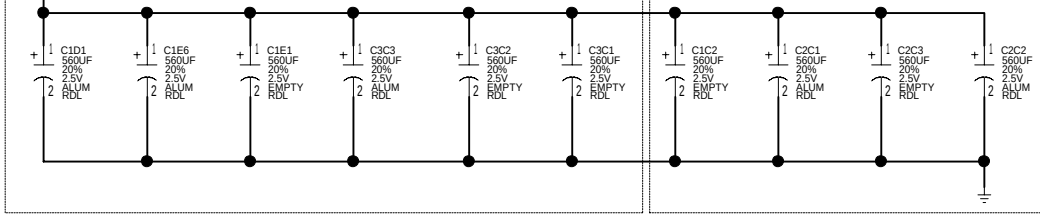
CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

644066-024

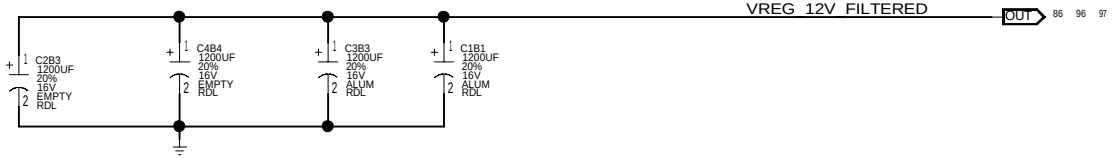


PLACEMENT NOTE FOR 1206:
PLACE 18 INSIDE CPU SOCKET (STUFF ALL)

CAD NOTE:
PLACE ON TOP (NORTH SIDE) OF SOCKET



CAD NOTE:
PLACE ON EAST SIDE OF SOCKET



[PAGE_TITLE=VCCP VREG DECOUPLING]

CORE PAGE

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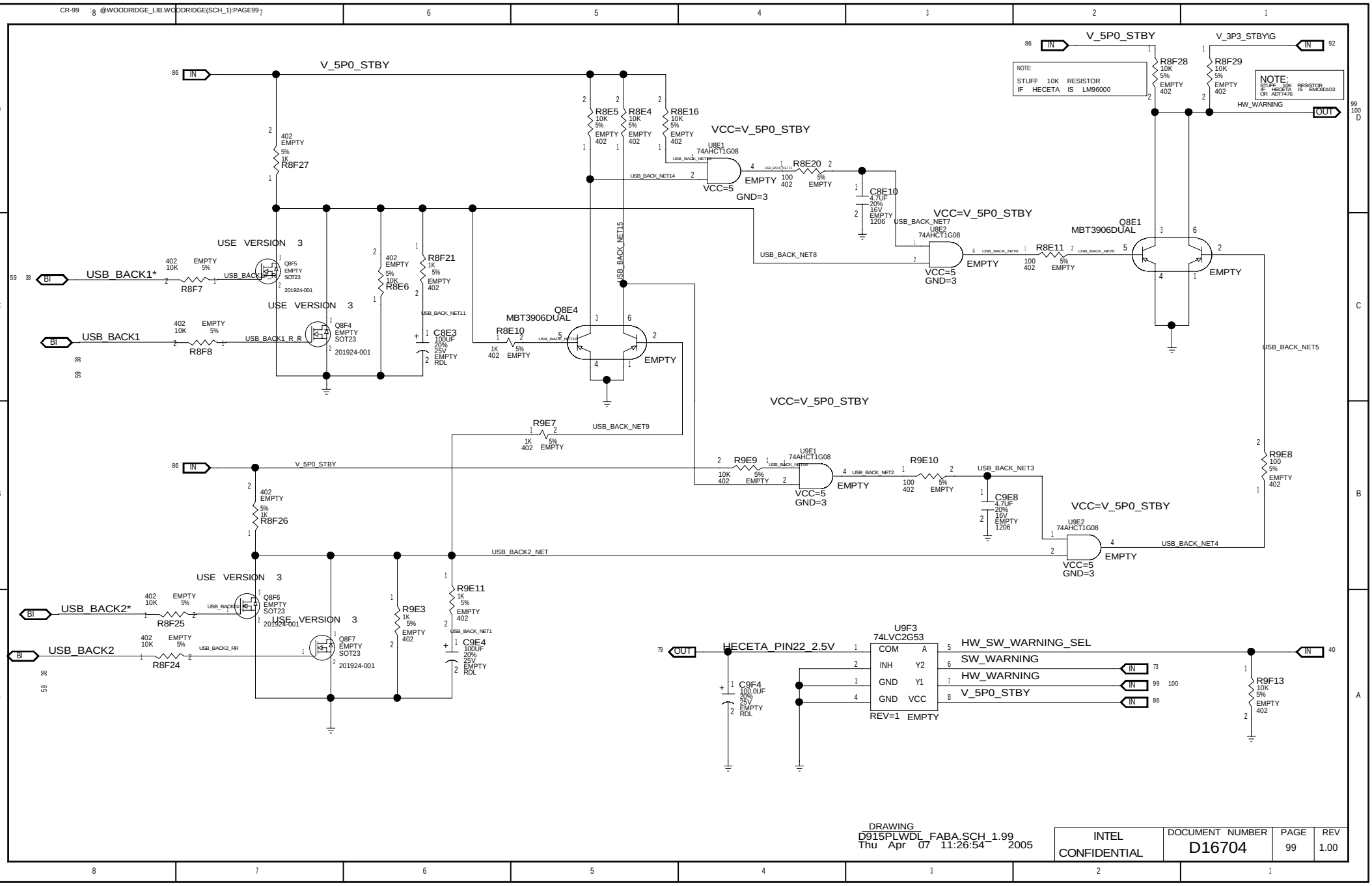
D915PLWDL_FABA.SCH_1.98
Thu Apr 07 13:44:41 2005



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D915PLWDL_FABA.SCH_1.99
Thu Apr 07 11:26:54 2005

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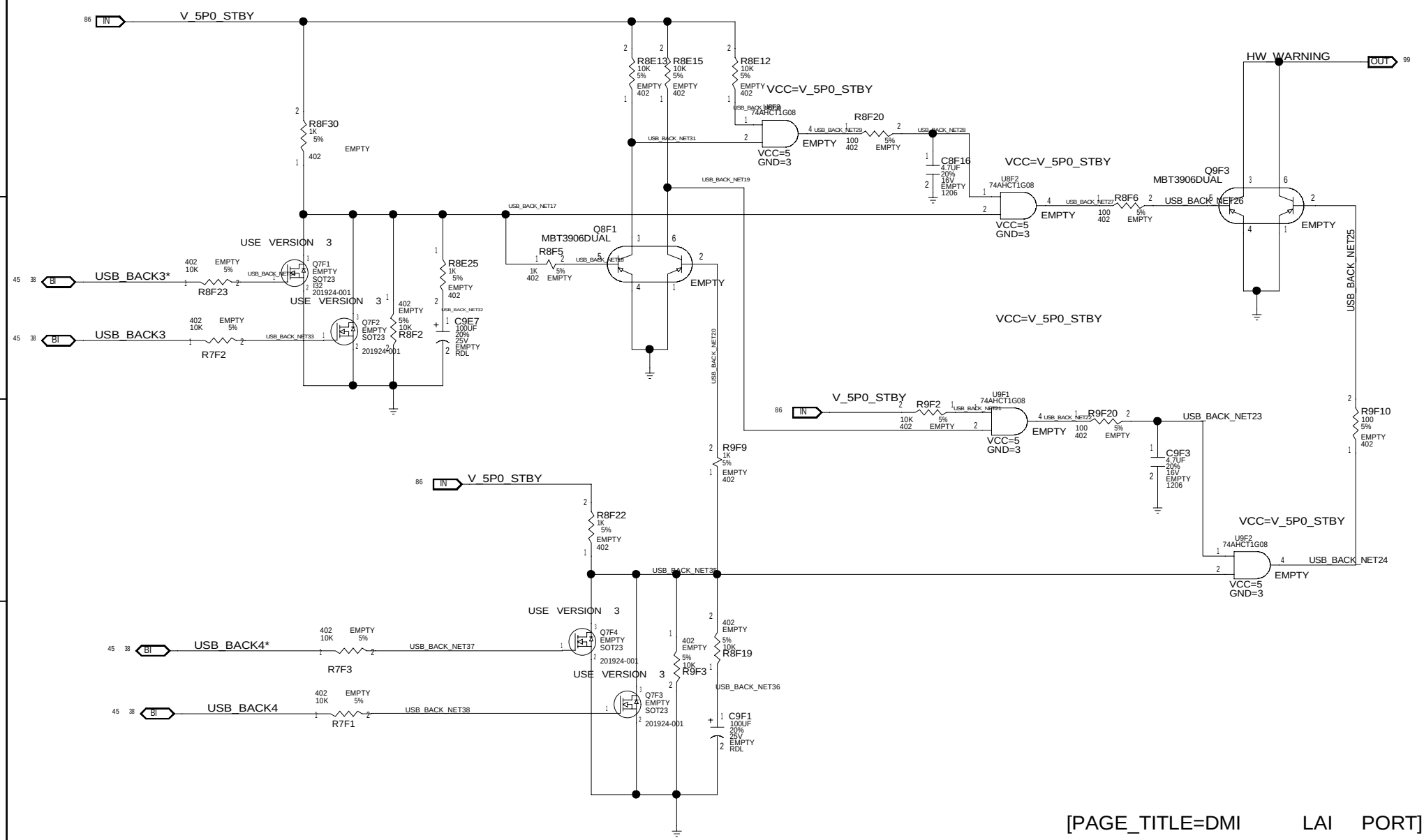
	D16704	99	1.00

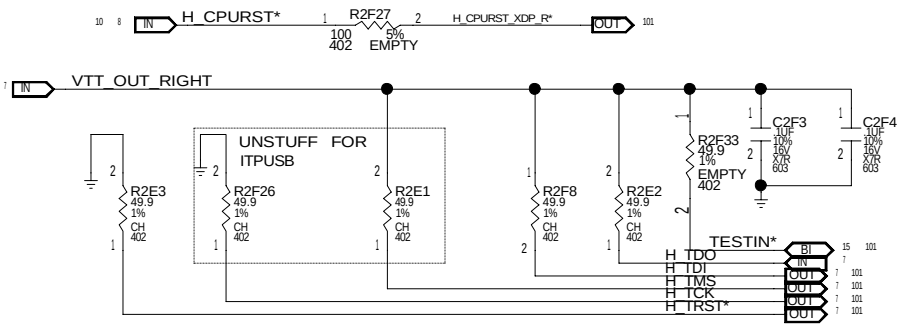


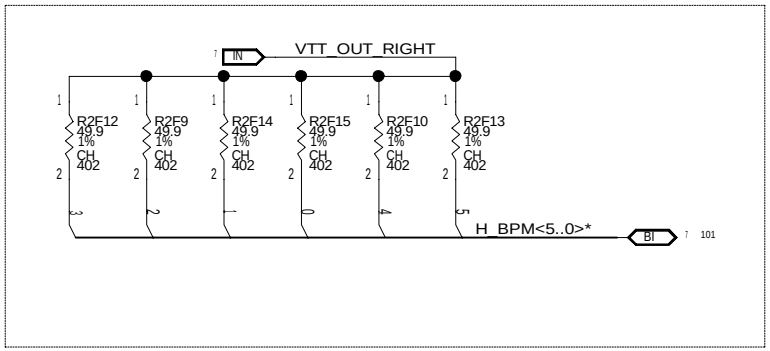
CORE PAGE

DMI = DIRECT MEDIA INTERFACE

DRAWING
D915PLWDL_FABA.SCH_1.100
Wed Apr 06 22:21:25 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	100	1.00



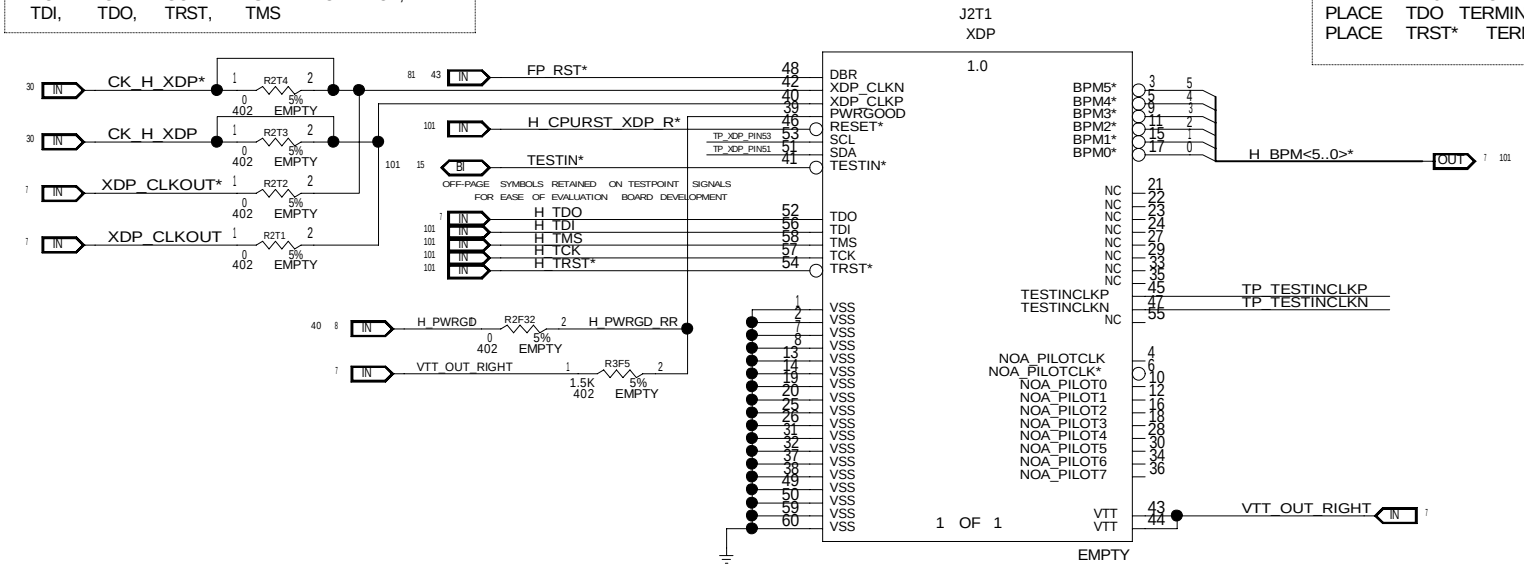


CAD NOTES:

XTG ROUTING RULES:
NOA MATCH LENGTHS WITHIN 50PS *
BPM MATCH LENGTHS WITHIN 50PS *
IDEALLY INCLUDE PACKAGE LENGTHS
NO LENGTH GUIDELINES FOR TCK, TDI, TDO, TRST, TMS

CAD NOTES:

PLACE BPM TERMINATION NEAR CONNECTOR
PLACE TCK/TDI TERMINATION NEAR CPU
WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.
PLACE TDO TERMINATION NEAR CONNECTOR
PLACE TRST* TERMINATION ANYWHERE ON ROUTE



XDP

CORE PAGE

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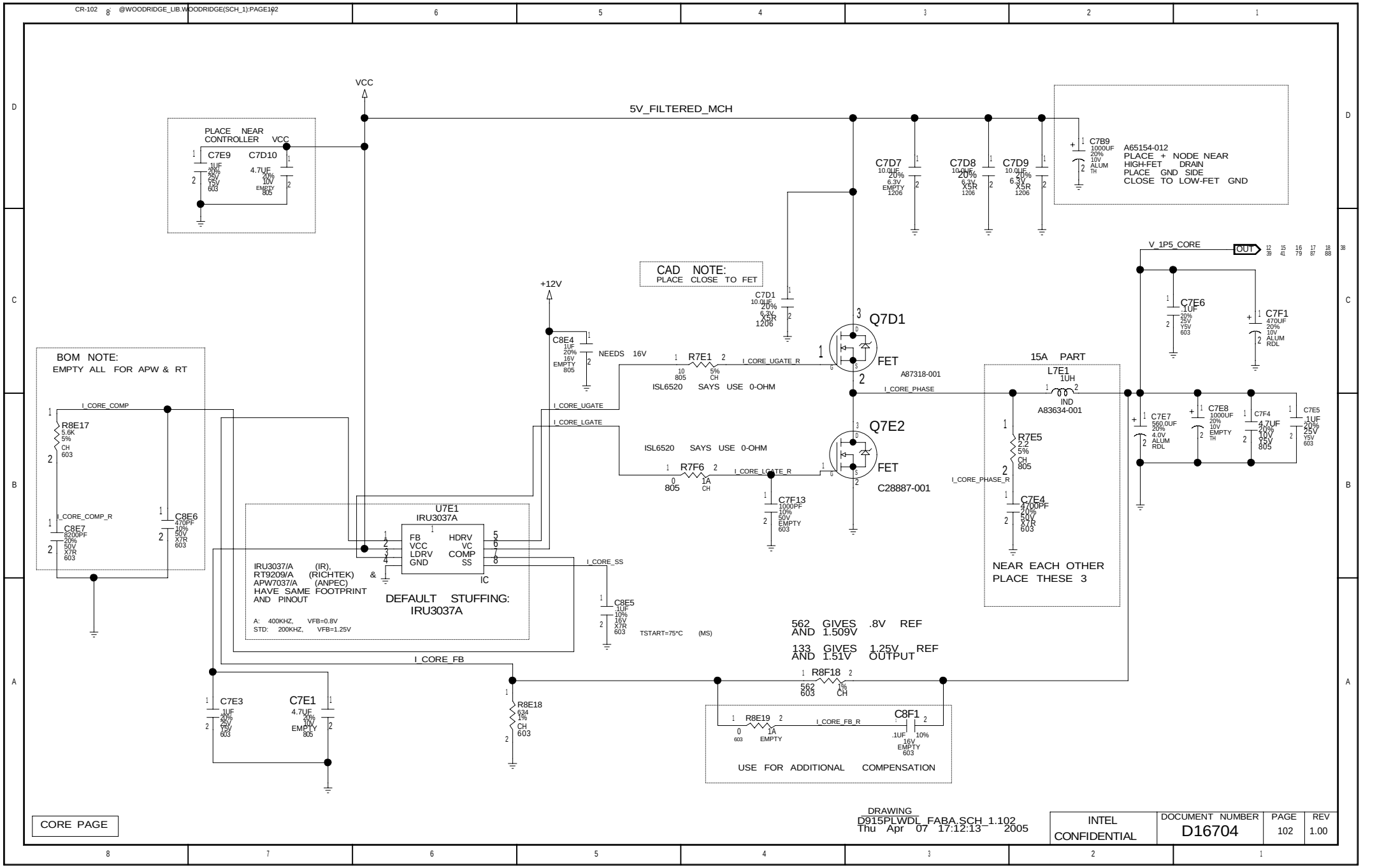
D915PLWDL_FABA_SCH_1.101
Thu Apr 07 00:59:02 2005

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	D16704	101	1.00


CR-102 @WOODRIDGE_LIB.WOODRIDGE(SCH_1):PAGE102
VCC
5V_FILTERED_MCH
PLACE NEAR CONTROLLER VCC
C7E9 1UF 20% 25V Y5V 603
C7D10 4.7UF 20% 10V EMPTY 805
C7D7 10.0UF 20% 6.3V EMPTY 1206
C7D8 10.0UF 20% 6.3V X5R 1206
C7D9 10.0UF 20% 6.3V X5R 1206
C7B9 1000UF 20% 10V ALUM TH
A65154-012
PLACE + NODE NEAR HIGH-FET DRAIN
PLACE GND SIDE CLOSE TO LOW-FET GND
CAD NOTE:
PLACE CLOSE TO FET
+12V
C7D1 10.0UF 20% 6.3V X5R 1206
C8E4 1UF 20% 16V EMPTY 805
NEEDS 16V
R7E1 10 805 5% CH
I_CORE_UGATE_R
Q7D1
FET
A87318-001
ISL6520 SAYS USE 0-OHM
I_CORE_PHASE
I_CORE_UGATE
I_CORE_LGATE
Q7E2
FET
C28887-001
R7F6 0 805 1A CH
I_CORE_LGATE_R
C7F13 1000PF 10% 50V EMPTY 603
15A PART
L7E1 1UH IND A83634-001
R7E5 2.2 5% CH 805
I_CORE_PHASE_R
C7E4 4700PF 20% 50V X7R 603
NEAR EACH OTHER PLACE THESE 3
V_1P5_CORE
OUT
C7E6 .1UF 20% 25V Y5V 603
C7F1 470UF 20% 10V ALUM RDL
C7E7 560.0UF 20% 4.0V ALUM RDL
C7E8 1000UF 20% 10V EMPTY TH
C7F4 4.7UF 20% 10V Y5V 805
C7E5 1UF 20% 25V Y5V 603
BOM NOTE:
EMPTY ALL FOR APW & RT
I_CORE_COMP
R8E17 5.6K 5% CH 603
I_CORE_COMP_R
C8E7 6200PF 20% 50V X7R 603
C8E6 470PF 10% 50V X7R 603
U7E1
IRU3037A
FB
VCC
LDRV
GND
HDRV
VC
COMP
SS
IC
IRU3037/A (IR),
RT9209/A (RICHTEK) &
APW7037/A (ANPEC)
HAVE SAME FOOTPRINT
AND PINOUT
DEFAULT STUFFING:
IRU3037A
A: 400KHZ, VFB=0.8V
STD: 200KHZ, VFB=1.25V
I_CORE_SS
C8E5 1UF 10% 16V X7R 603
TSTART=75*C (MS)
562 GIVES .8V REF
AND 1.509V
133 GIVES 1.25V REF
AND 1.51V OUTPUT
I_CORE_FB
C7E3 .1UF 20% 25V Y5V 603
C7E1 4.7UF 20% 10V EMPTY 805
R8E18 634 1% CH 603
R8F18 562 603 1% CH
R8E19 0 603 1A EMPTY
I_CORE_FB_R
C8F1 .1UF 10% 16V EMPTY 603
USE FOR ADDITIONAL COMPENSATION
CORE PAGE
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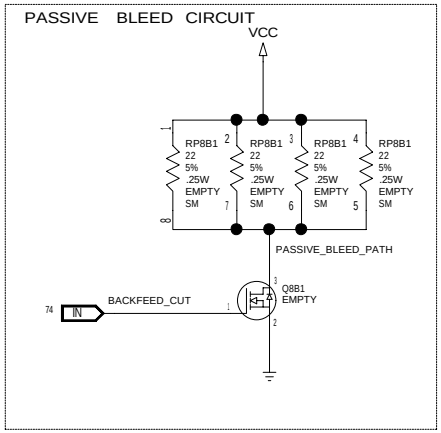
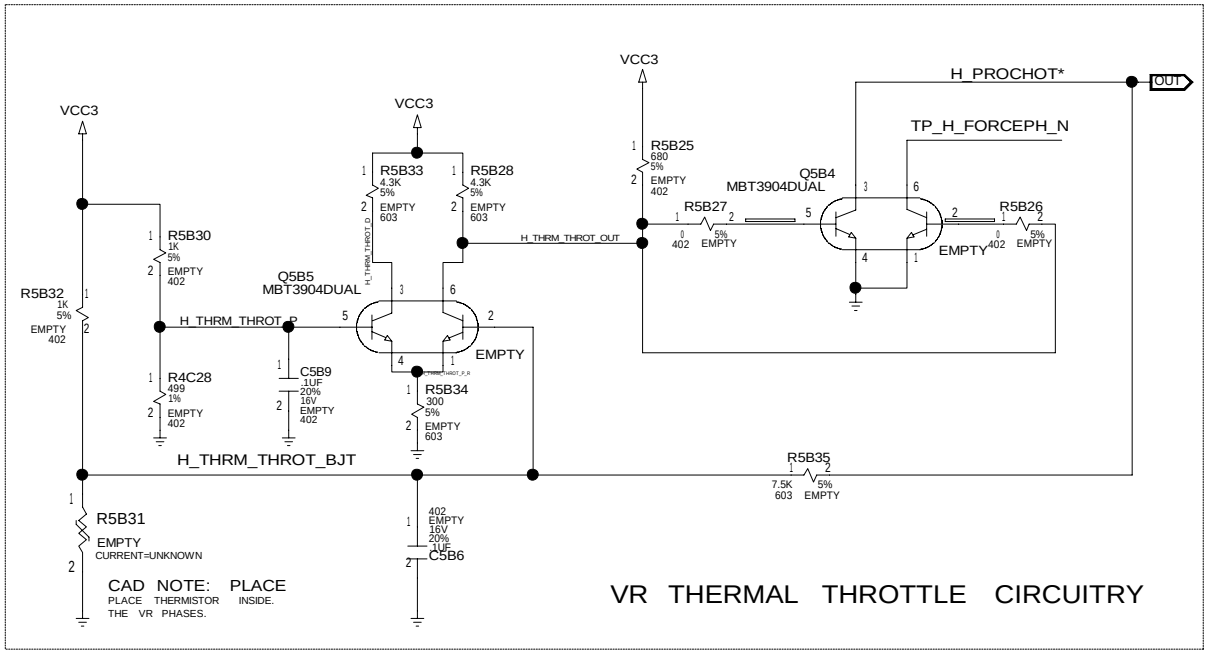
1.00





[PAGE_TITLE=THERMAL THROTTLE AND PASSIVE BLEED]

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Thu Apr 07 01:00:02 2005

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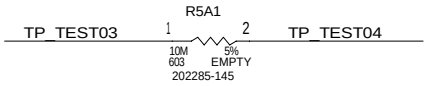
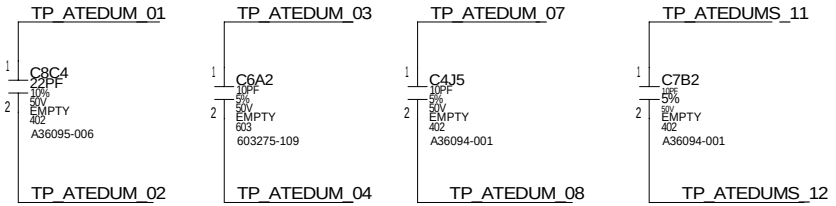
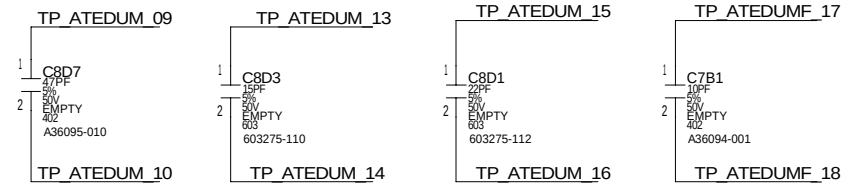
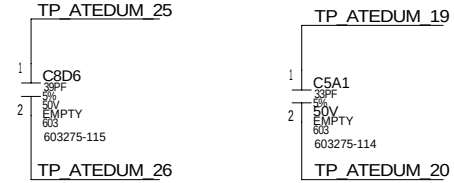
	D16704	103	1.00

TEST SITE









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D915PLWDL_FABA.SCH_1.104
Thu Apr 07 00:58:44 2005

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	D16704	104	1.00

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