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PGA462 Socket A CPU0/CPU1	4,5,6,7
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MS-6501 ATX

**Version
0A**

Last Update xx/xx/2000

**CPU:
Dual AMD Socket-462 Processors**

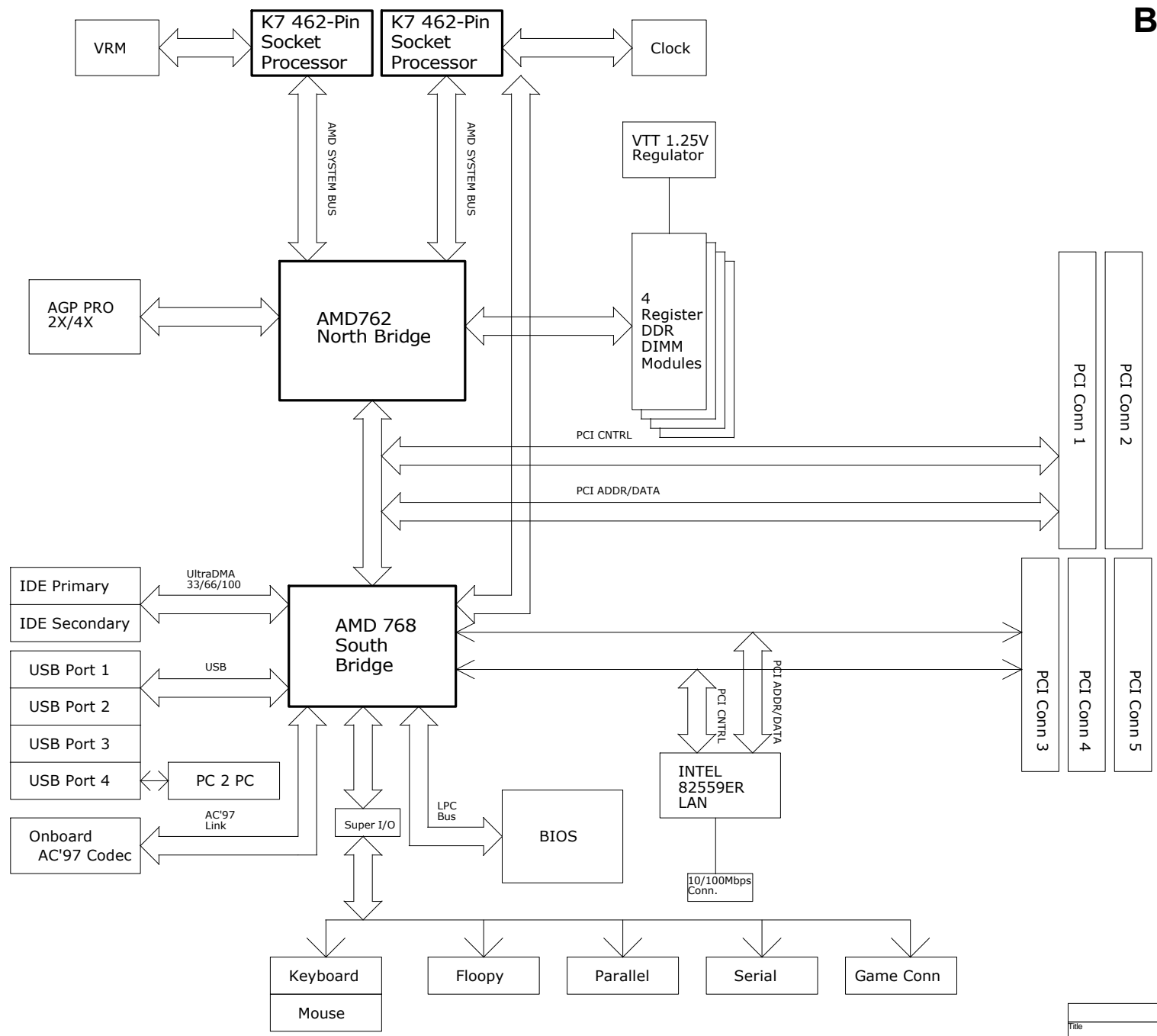
**System Chipset:
AMD 762(North Bridge)
AMD 768 (South Bridge)**

**Expansion Slots:
AGP-Pro SLOT * 1
PCI2.2 PCI/64/66 SLOT * 2
PCI2.2 PCI/32/33 SLOT * 3**

**On Board:
LAN 82559ER
AC97 Codec
PC 2 PC**

MICRO-STAR			
Title Cover Sheet			
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Block Diagram

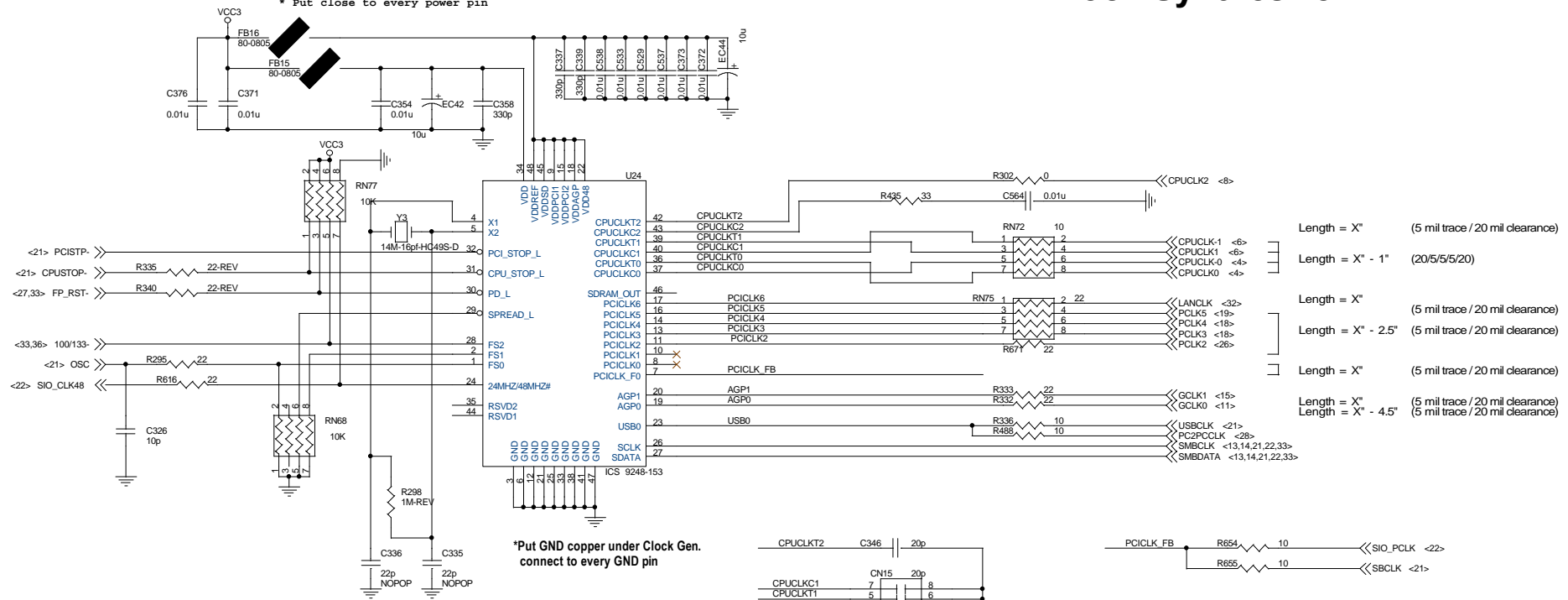


MICRO-STAR			
Title			
Block Diagram			
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Clock Synthesizer

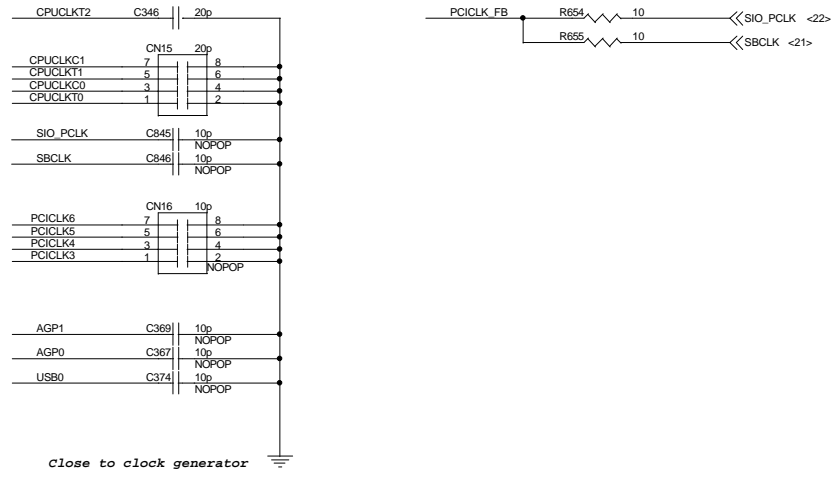
* 25 mils Trace on Layer 6
with GND copper around it

* Put close to every power pin



- Length = X" (5 mil trace / 20 mil clearance)
- Length = X" - 1" (20/5/5/20)
- Length = X" (5 mil trace / 20 mil clearance)
- Length = X" - 2.5" (5 mil trace / 20 mil clearance)
- Length = X" (5 mil trace / 20 mil clearance)
- Length = X" (5 mil trace / 20 mil clearance)
- Length = X" - 4.5" (5 mil trace / 20 mil clearance)

*Put GND copper under Clock Gen.
connect to every GND pin



Close to clock generator

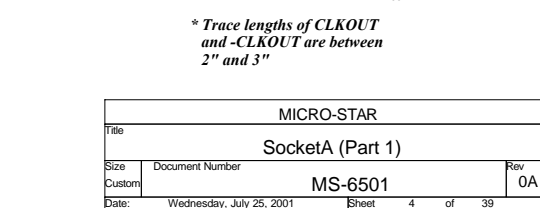
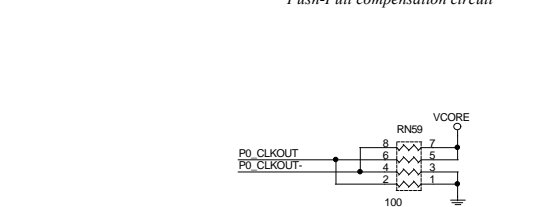
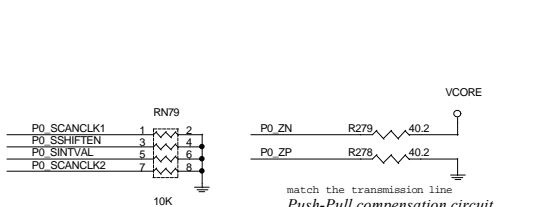
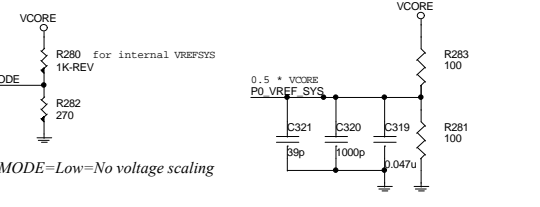
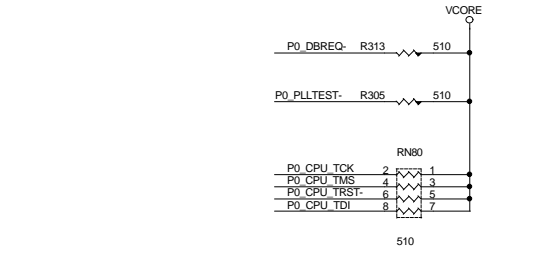
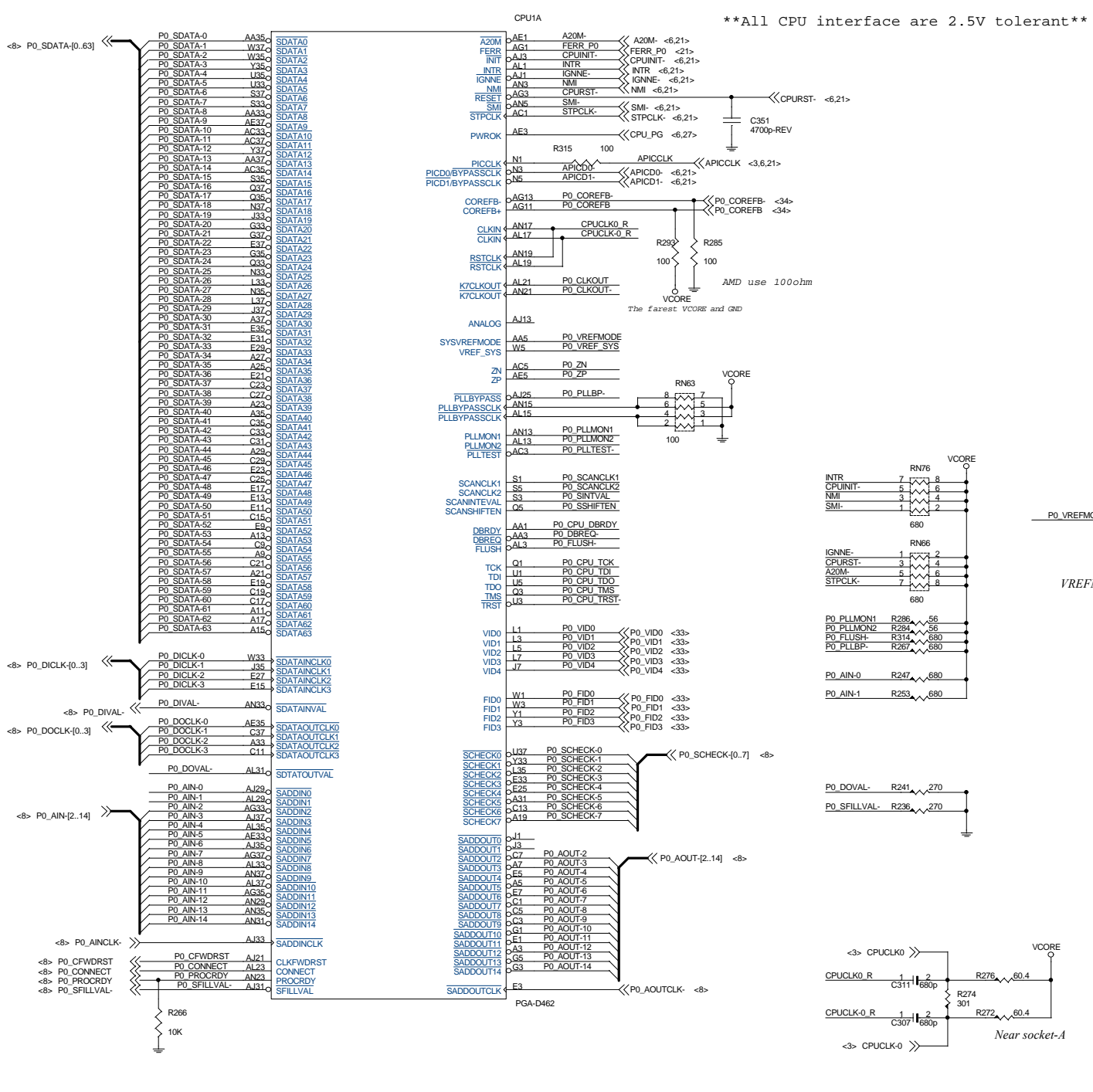
	WIDTH/SPACE	LENGTH
CPUCLK0&CPUCLK0#:	5/20 5 FOR DIFF. PAIR	X-1 INCH
CPUCLK1&CPUCLK1#:	5/20 5 FOR DIFF. PAIR	X-1 INCH
CPUCLK2&GCLK0	5/20	X
GCLK1	5/20	X-4.5
NBCLK&SBCLK	5/20	X
PCICLK GROUP	5/20	X-2.5

	FS2	FS1	FS0	GPU SDRAM	PCI	AGP
	0	0	0	133.3	33.3	66.7
	0	0	1	95.0	31.67	63.33
	0	1	0	100.99	33.66	67.33
	0	1	1	115.0	38.33	76.67
	1	0	0	100.7	33.57	67.13
	1	0	1	103.0	34.33	66.6
	1	1	0	105.0	35.00	60.0
	1	1	1	110.0	36.67	66.6

* X MEANS THE SHORTEST LENGTH FOR MAINTAIN
PROPAGATION DELAY

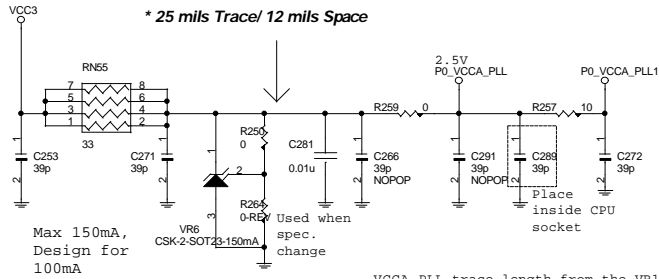
* CPUCLK1'S TERMINATION CKT MUST BE PLACED
NEAR TO NB

MICRO-STAR		
Title Clock Synthesizer		
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** Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"*

MICRO-STAR		
SocketA (Part 1)		
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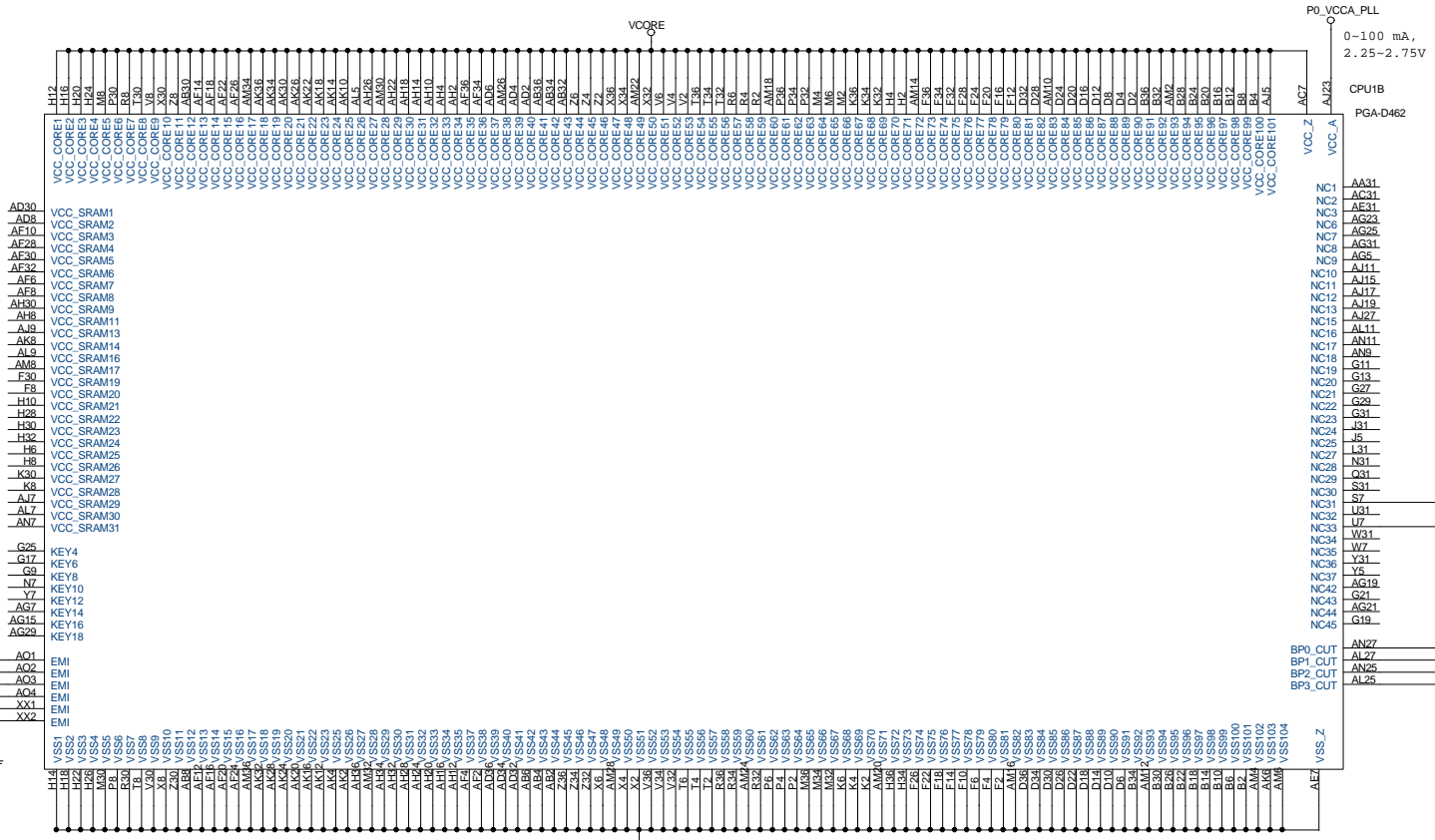


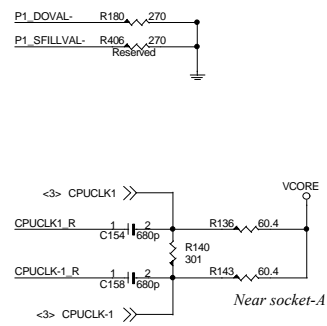
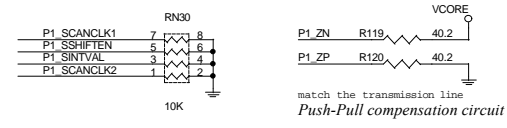
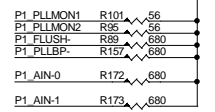
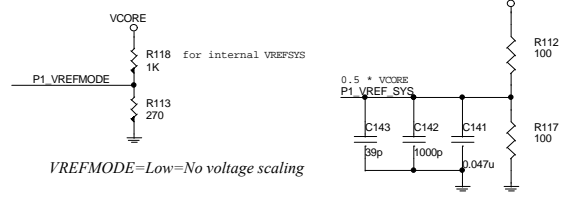
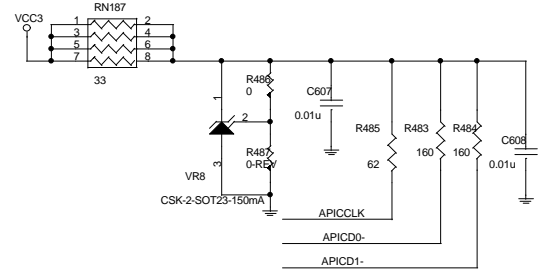
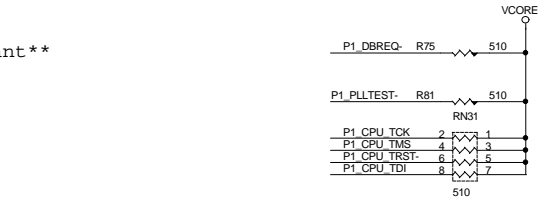
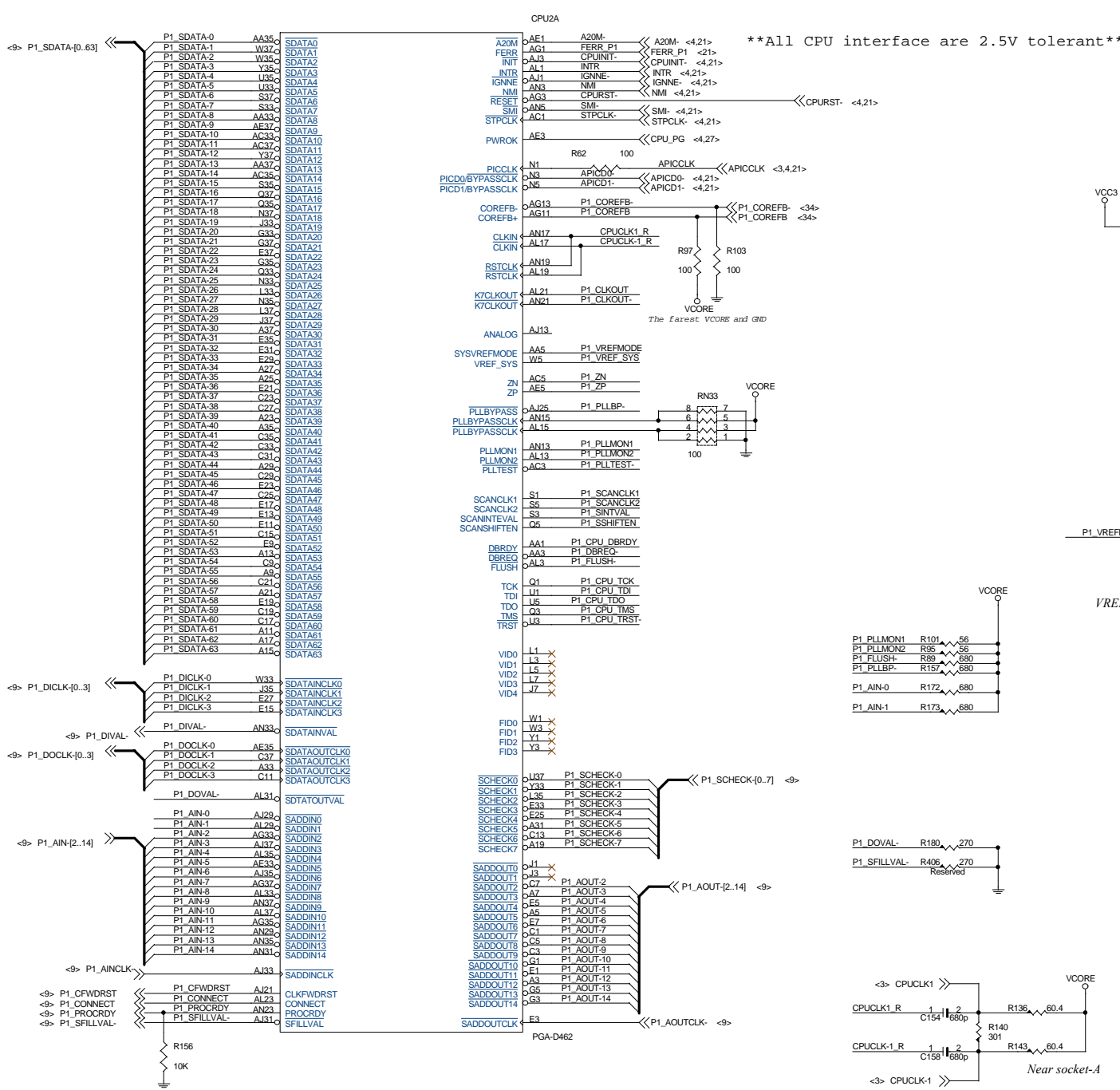
Power Up Strappings :

AD[3:0] => CPU Clock Multiplier

0000	3	1000	7
0001	3.5	1001	7.5
0010	4	1010	8
0011	4.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	Reserved

VCCA_PLL trace length from the VR1 to the PGA must be 0.75".
 Place all filters close to the PGA.
 Keep all power and signal trace away from the VR1.
 Place a cut in the GND plane around the VCCA_PLL regulator circuit.

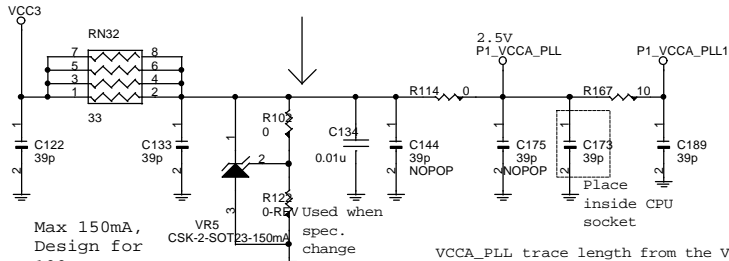




* Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"

MICRO-STAR		
SocketA (Part 1)		
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* 25 mils Trace/ 12 mils Space



Max 150mA,
Design for
100mA

VCCA_PLL trace length from the VR1 to the
PGA must be 0.75".

Place all filters close to the PGA.

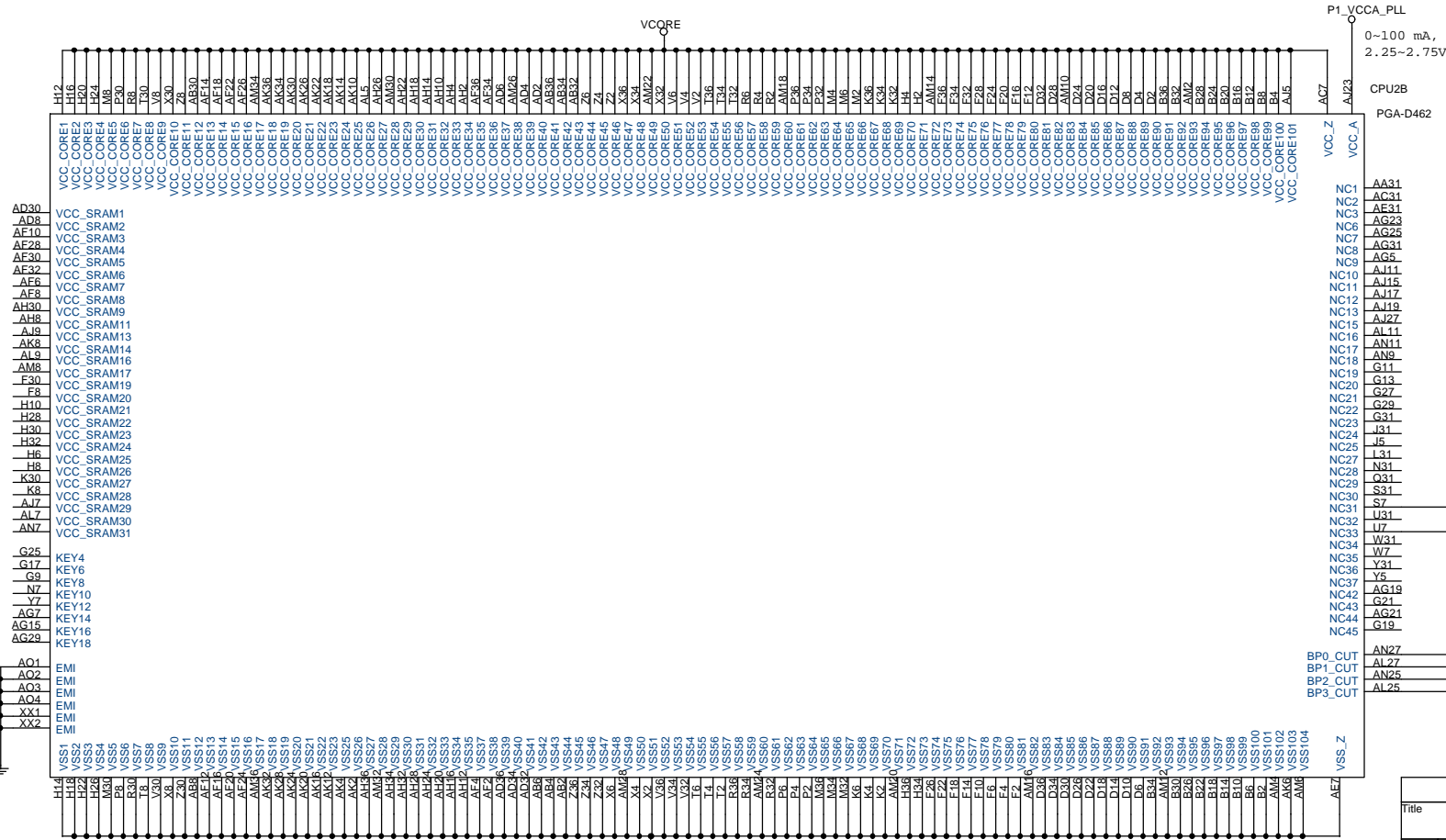
Keep all power and signal trace away from
the VR1.

Place a cut in the GND plane around the
VCCA_PLL regulator circuit.

Power Up Strappings :

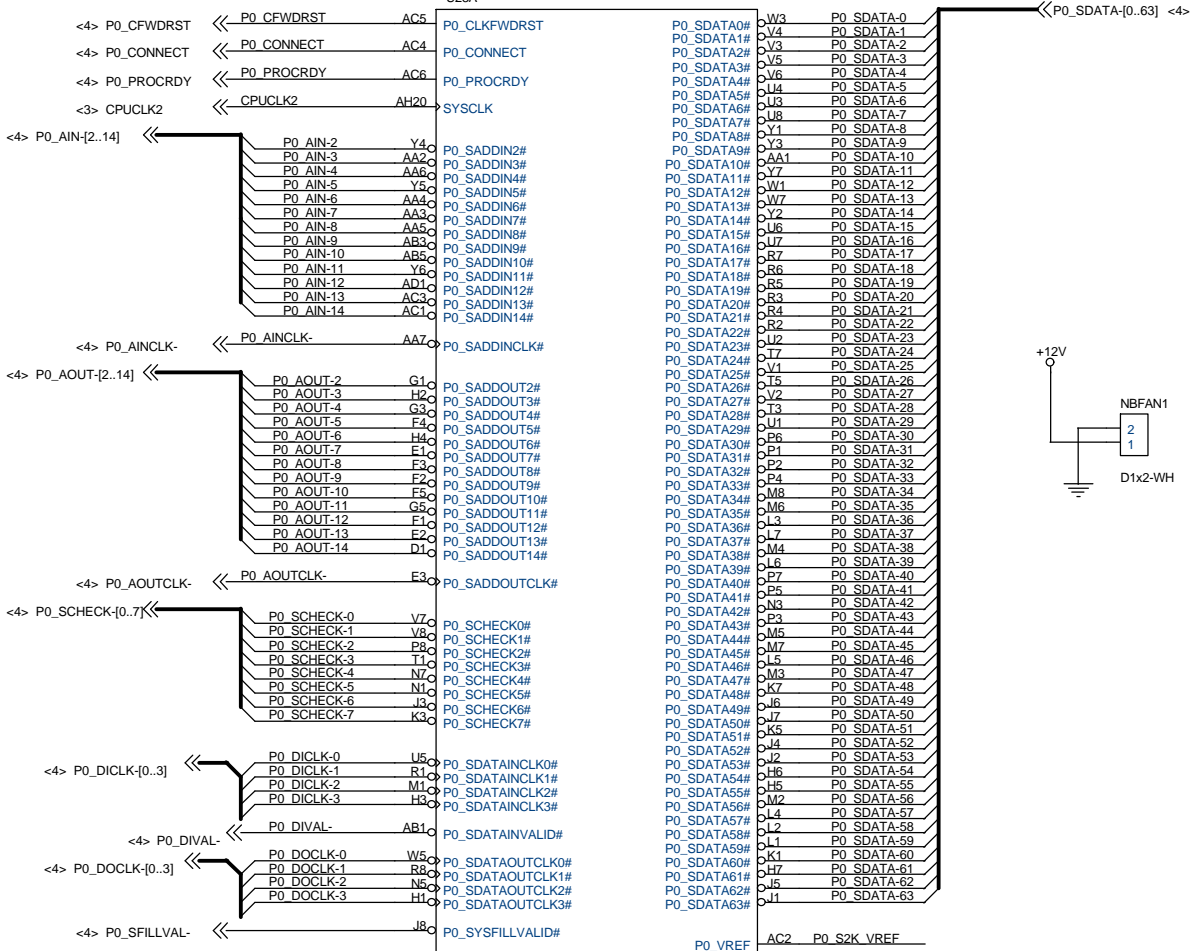
AD[3:0] => CPU Clock Multiplier

0000	3	1000	7
0001	3.5	1001	7.5
0010	4	1010	8
0011	4.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	Reserved



MICRO-STAR			
SocketA (Part 2)			
Title	Document Number		Rev
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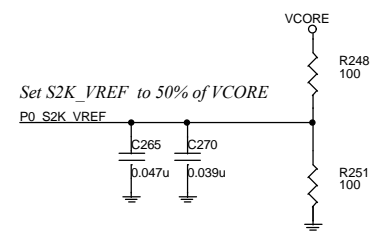
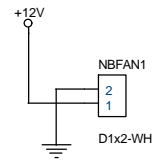
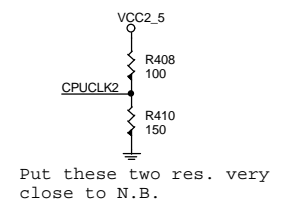
AMD-762
System Bus 0



BELONG TO CLKFWD GROUP[SADDIN] MATCH
W/IN +/-50MILS OF GROUP 5/10,
CLK:5/20

BELONG TO CLKFWD GROUP[SADDOUT] MATCH
W/IN +/-50MILS OF GROUP 5/10,
CLK:5/20

BELONG TO CLKFWD GROUP;MATCHED TO
INDIVIDUAL CLKFWD GROUP
RESPECTIVELY.[SDATA0], [SDATA1],
[SDATA2],[SDATA3] W/IN +/-50MILS OF
GROUP



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5

4

3

2

1

5

4

3

2

1

AMD-762
System Bus 1

U23B

D

C

B

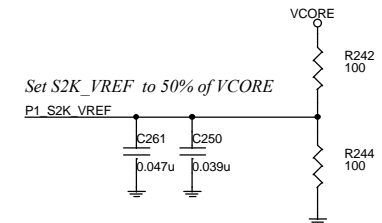
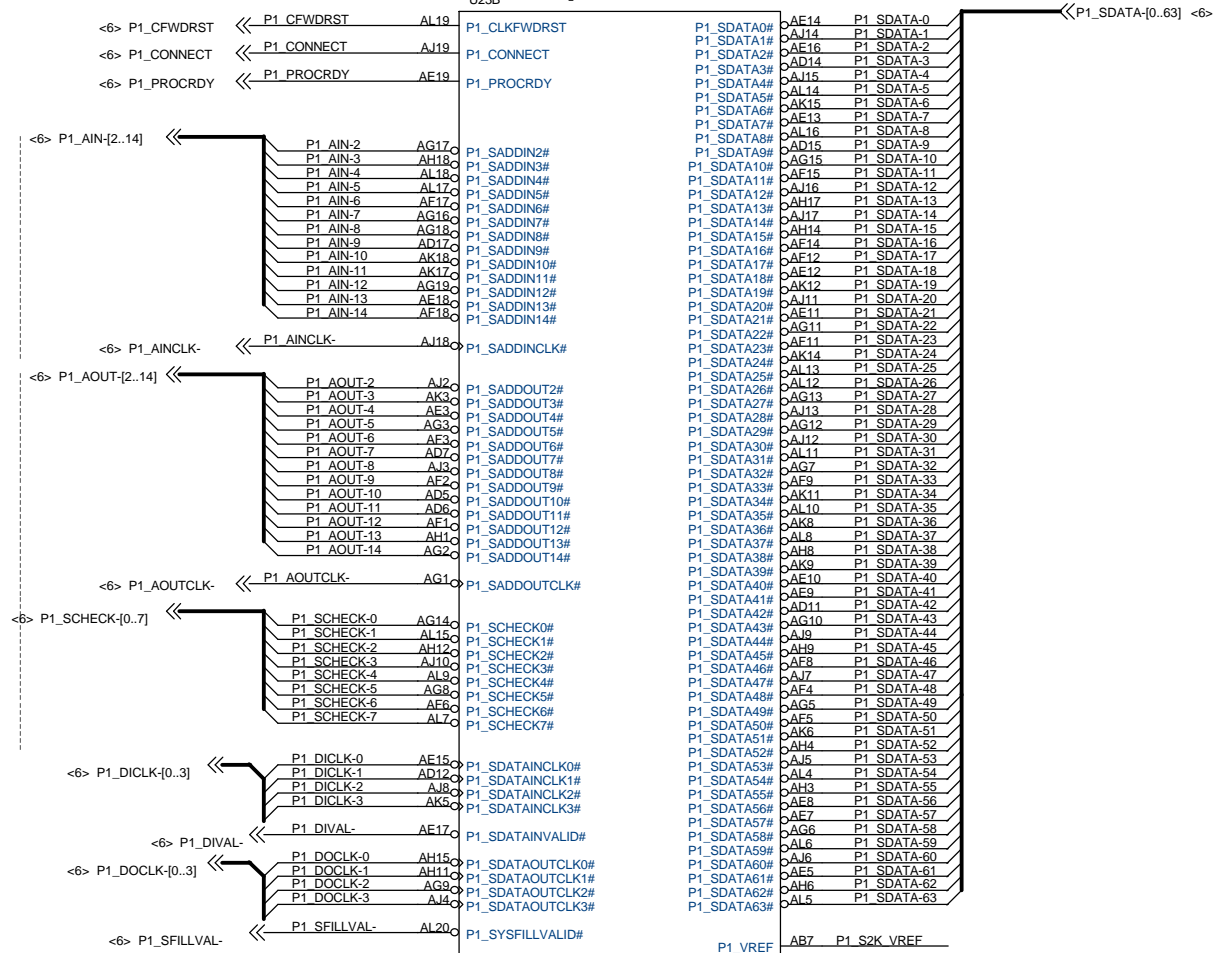
A

BELONG TO CLKFWD GROUP[SADDIN] MATCH
W/IN +/-50MILS OF GROUP 5/10,
CLK:5/20

BELONG TO CLKFWD GROUP[SADDOUT] MATCH
W/IN +/-50MILS OF GROUP 5/10,
CLK:5/20

BELONG TO CLKFWD GROUP;MATCHED TO
INDIVIDUAL CLKFWD GROUP

RESPECTIVELY.[SDATA0],[SDATA1],
[SDATA2],[SDATA3] W/IN +/-50MILS OF
GROUP



MICRO-STAR		
Title North Bridge AMD762-CPU1		
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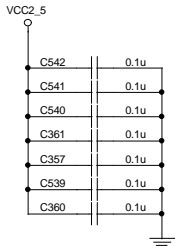
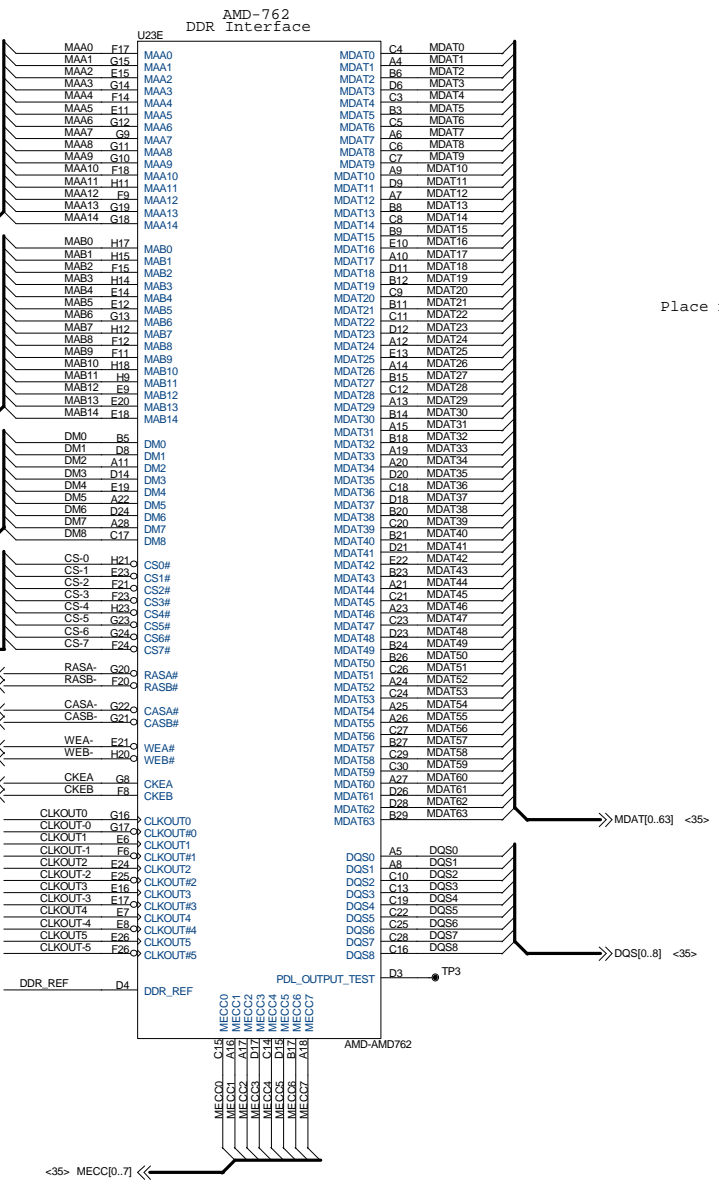
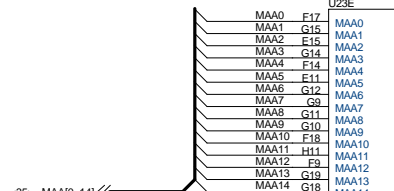
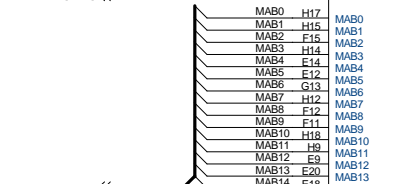
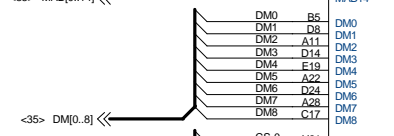
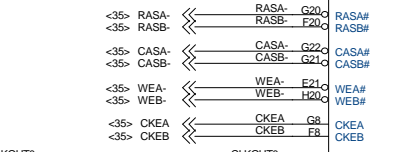
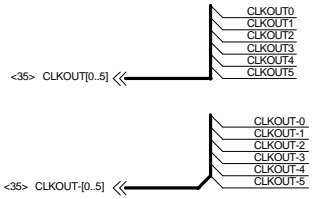
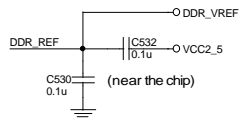
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4

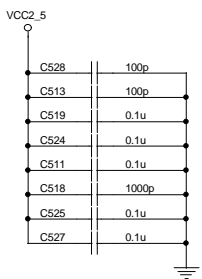
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2

1

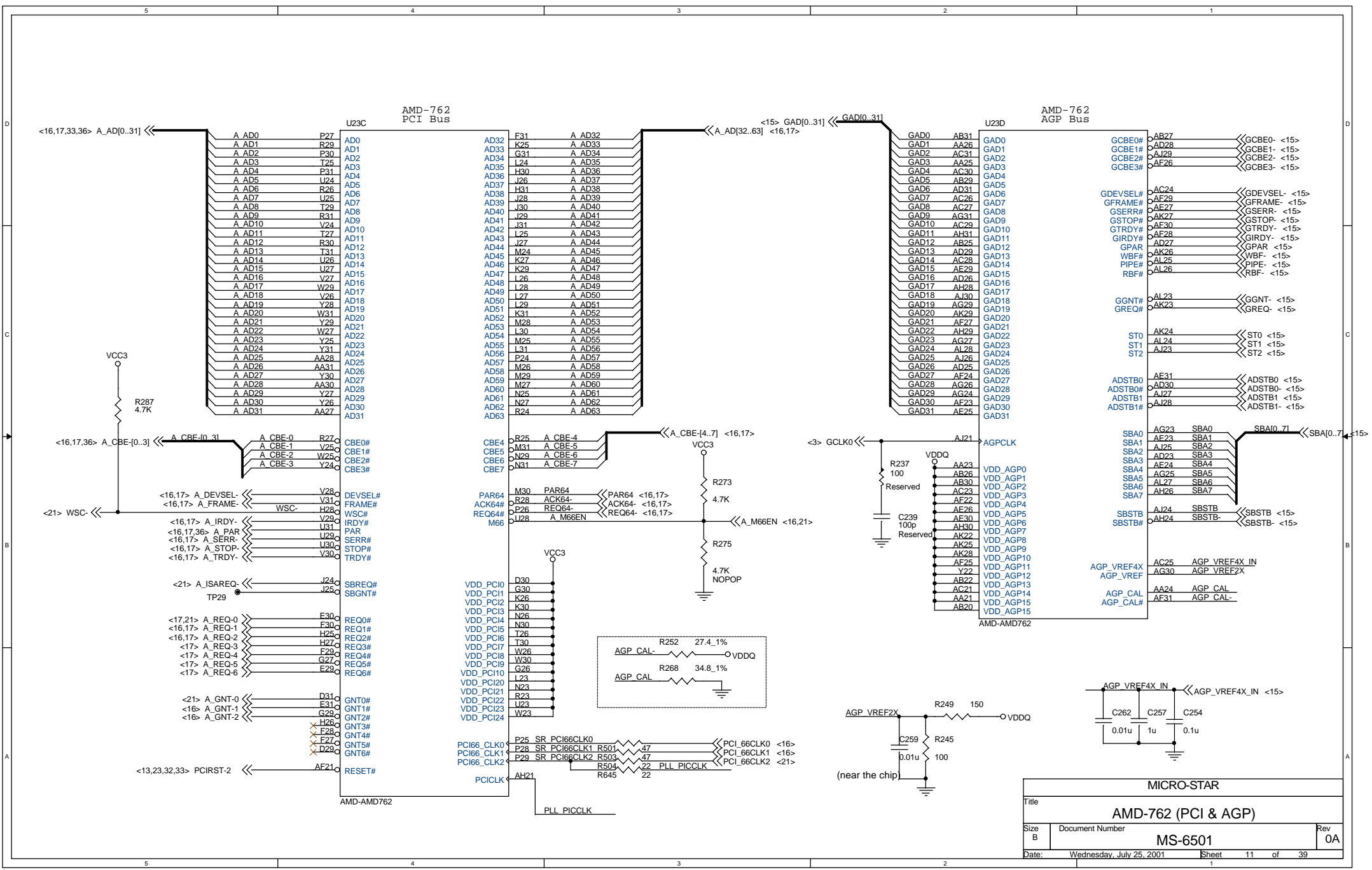


Place near IGD4 for VCC2_5 decoupling

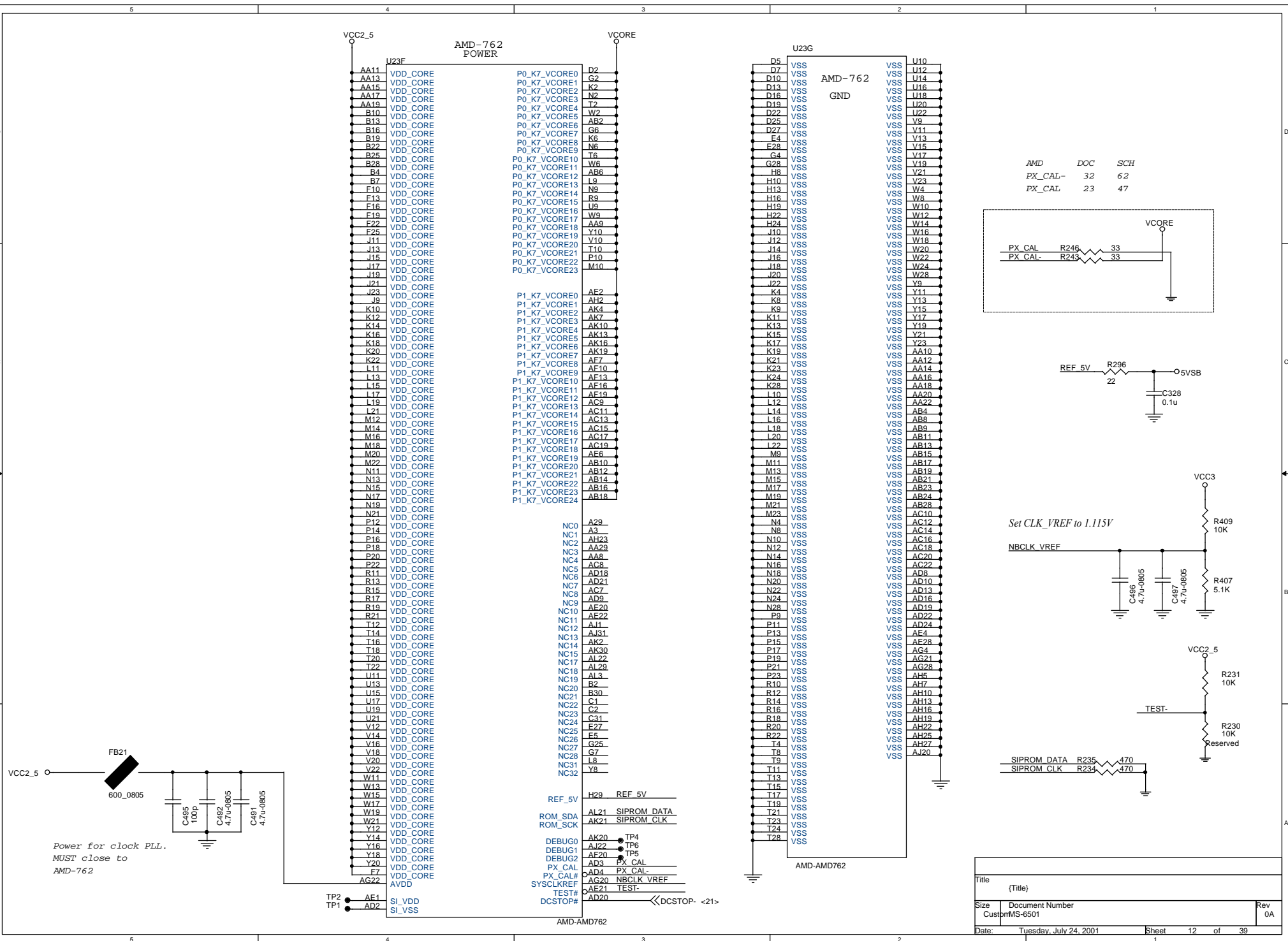


Place under IGD4 (NOPOP)

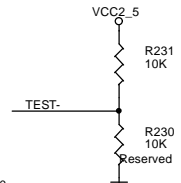
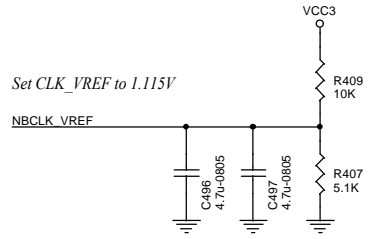
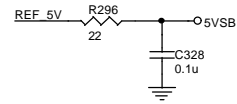
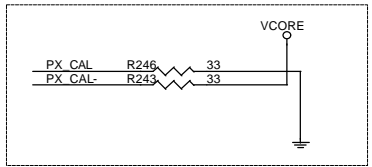
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Title		
North Bridge AMD762-DDR		
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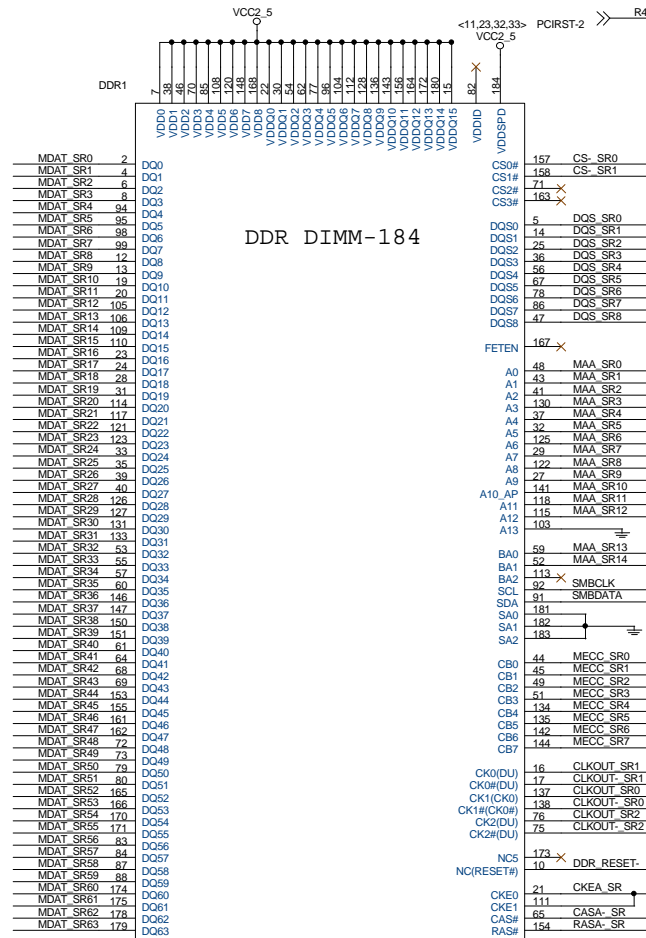
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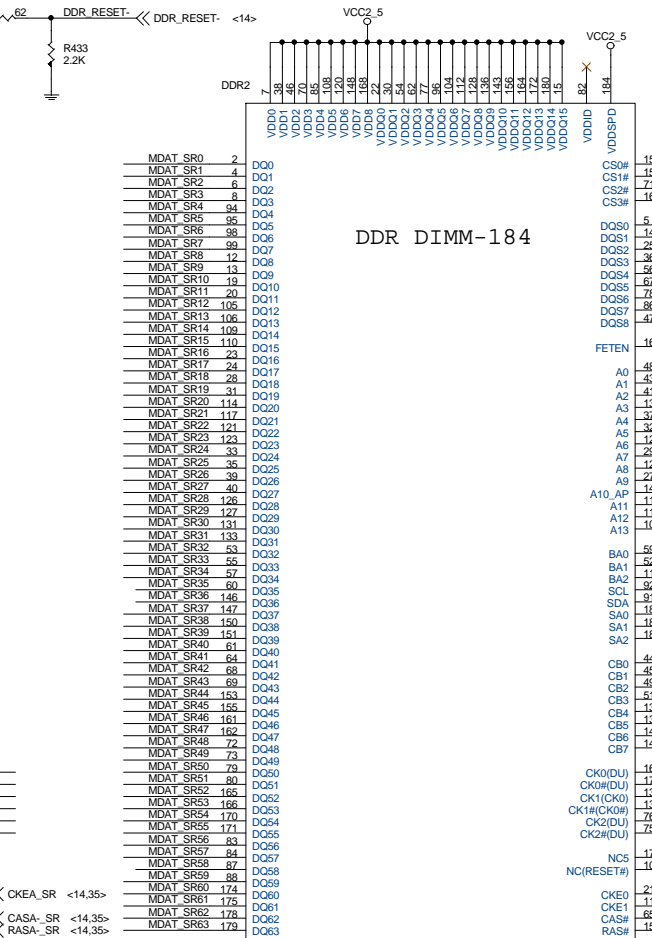
AMD	DOC	SCH
PX_CAL-	32	62
PX_CAL	23	47



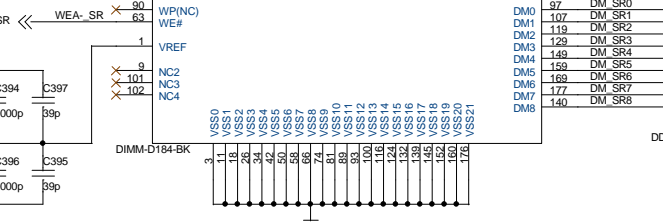
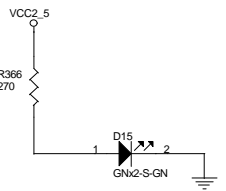
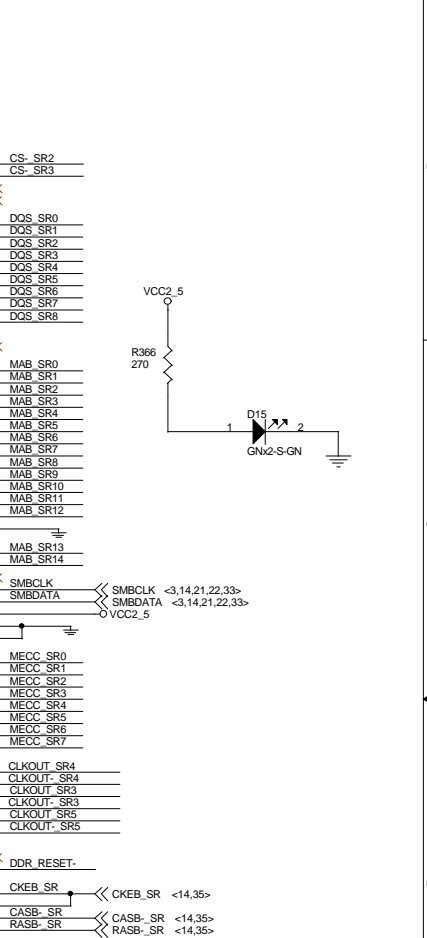
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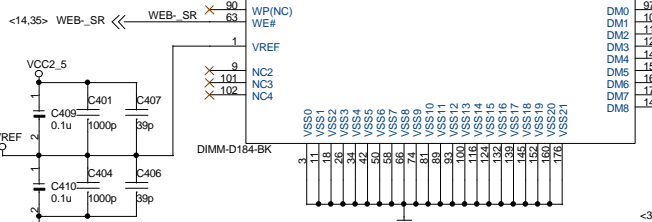
DDR DIMM-184



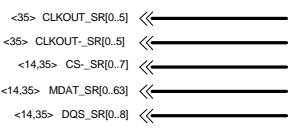
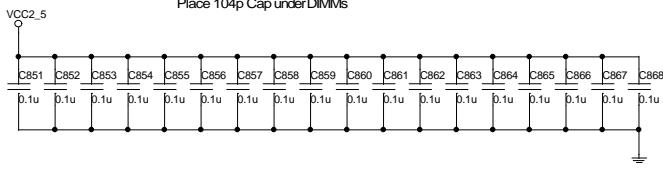
DDR DIMM-184

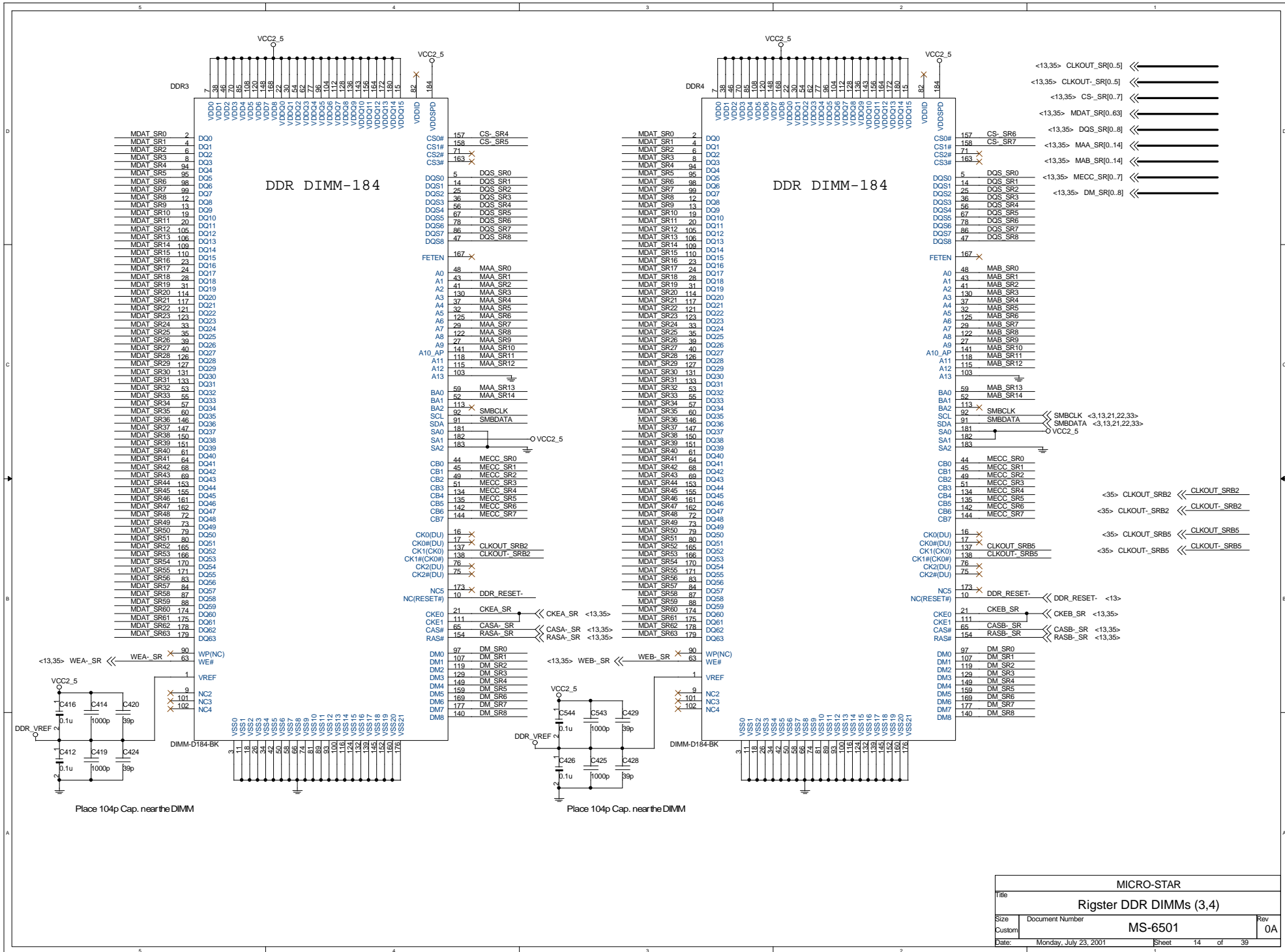


Place 104p Cap under DIMMs



Place 104p Cap. near the DIMM

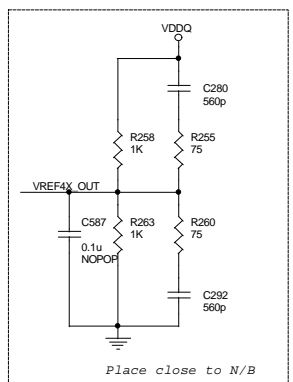
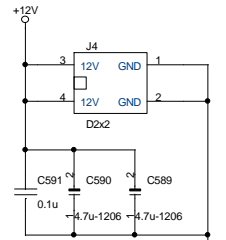
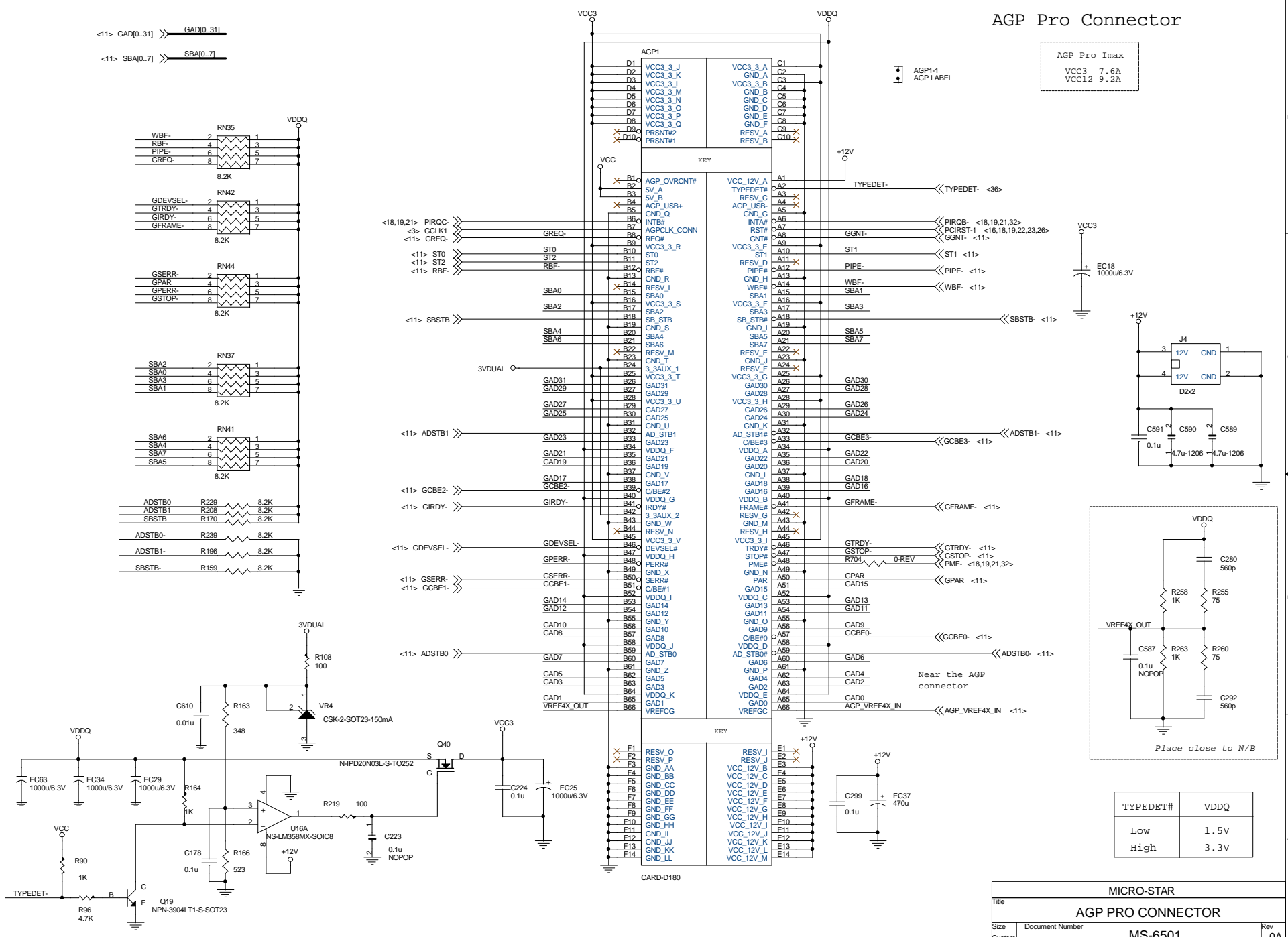




MICRO-STAR			
Title Rigster DDR DIMMs (3,4)			
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AGP Pro Connector

AGP Pro Imax
VCC3 7.6A
VCC12 9.2A



TYPEDET#	VDDQ
Low	1.5V
High	3.3V

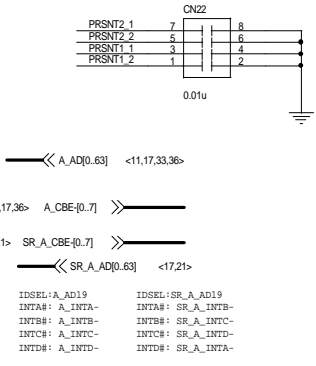
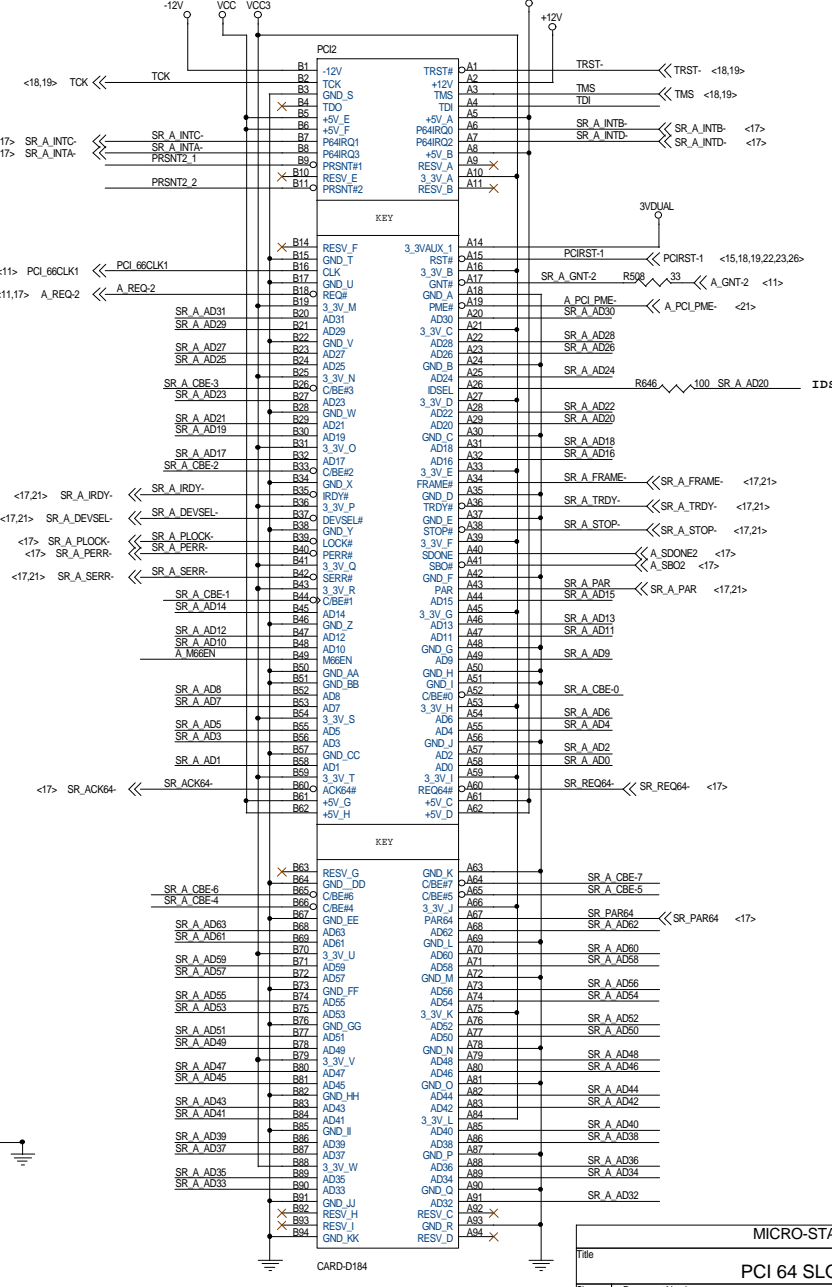
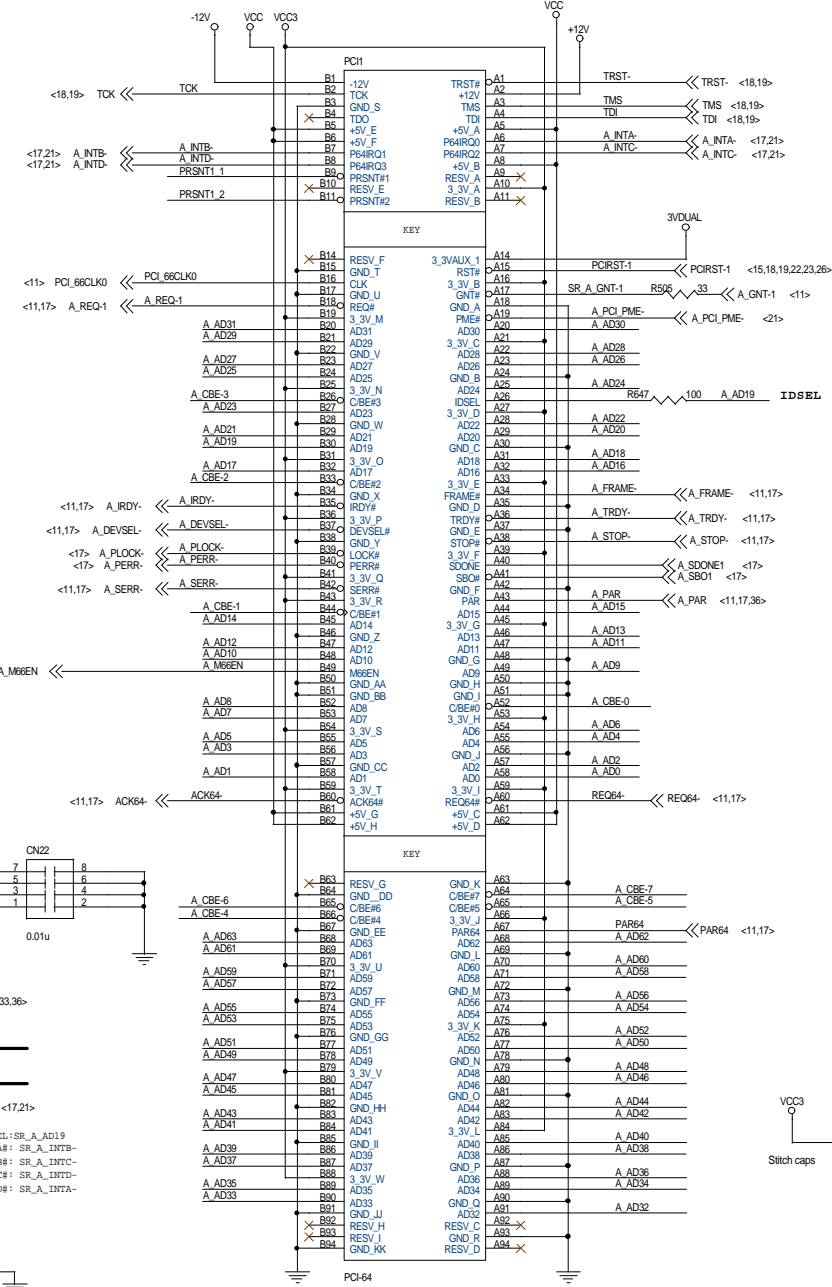
MICRO-STAR

Title: **AGP PRO CONNECTOR**

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PCI 64 SLOT



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RN218
A AD63 2 1 SR A AD63
A AD62 4 1 SR A AD62
A AD61 6 1 SR A AD61
A AD60 8 1 SR A AD60
33

RN222
A AD59 2 1 SR A AD59
A AD58 4 1 SR A AD58
A AD57 6 1 SR A AD57
A AD56 8 1 SR A AD56
33

RN226
A AD55 2 1 SR A AD55
A AD54 4 1 SR A AD54
A AD53 6 1 SR A AD53
A AD52 8 1 SR A AD52
33

RN229
A AD51 2 1 SR A AD51
A AD50 4 1 SR A AD50
A AD49 6 1 SR A AD49
A AD48 8 1 SR A AD48
33

RN233
A AD47 2 1 SR A AD47
A AD46 4 1 SR A AD46
A AD45 6 1 SR A AD45
A AD44 8 1 SR A AD44
33

RN236
A AD43 2 1 SR A AD43
A AD42 4 1 SR A AD42
A AD41 6 1 SR A AD41
A AD40 8 1 SR A AD40
33

RN237
A AD39 2 1 SR A AD39
A AD38 4 1 SR A AD38
A AD37 6 1 SR A AD37
A AD36 8 1 SR A AD36
33

RN240
A AD35 2 1 SR A AD35
A AD34 4 1 SR A AD34
A AD33 6 1 SR A AD33
A AD32 8 1 SR A AD32
33

RN243
A AD31 2 1 SR A AD31
A AD30 4 1 SR A AD30
A AD29 6 1 SR A AD29
A AD28 8 1 SR A AD28
33

RN246
A AD27 2 1 SR A AD27
A AD26 4 1 SR A AD26
A AD25 6 1 SR A AD25
A AD24 8 1 SR A AD24
33

RN249
A AD23 2 1 SR A AD23
A AD22 4 1 SR A AD22
A AD21 6 1 SR A AD21
A AD20 8 1 SR A AD20
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RN253
A AD18 2 1 SR A AD18
A AD19 4 1 SR A AD19
A AD16 6 1 SR A AD16
A AD17 8 1 SR A AD17
33

RN257
A AD15 2 1 SR A AD15
A AD14 4 1 SR A AD14
A AD13 6 1 SR A AD13
A AD12 8 1 SR A AD12
33

RN261
A AD11 2 1 SR A AD11
A AD9 4 1 SR A AD9
A AD10 6 1 SR A AD10
A AD8 8 1 SR A AD8
33

RN264
A AD7 2 1 SR A AD7
A AD6 4 1 SR A AD6
A AD5 6 1 SR A AD5
A AD4 8 1 SR A AD4
33

RN267
A AD3 2 1 SR A AD3
A AD1 4 1 SR A AD1
A AD2 6 1 SR A AD2
A AD0 8 1 SR A AD0
33

<11,16> A_SERR- R662 33 SR A_SERR- <16,21>
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<11,16> PAR64 R665 33 SR_PAR64 <16>

RN221
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A_CBE-0 R666 33 SR A_CBE-0
A_CBE-1 R667 33 SR A_CBE-1
A_CBE-2 R668 33 SR A_CBE-2
A_CBE-3 R669 33 SR A_CBE-3

RN228
A_CBE-7 2 1 SR A_CBE-7
A_CBE-6 4 1 SR A_CBE-6
A_CBE-5 6 1 SR A_CBE-5
A_CBE-4 8 1 SR A_CBE-4

RN231
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<11,16> A_DEVSEL- 4 1 SR A_DEVSEL- <16,21>
<16> A_PLOCK- 6 1 SR A_PLOCK- <16>
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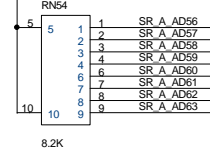
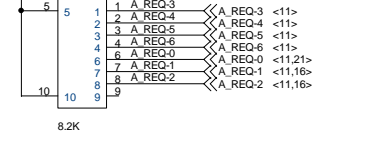
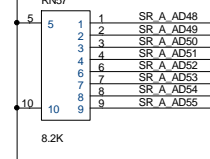
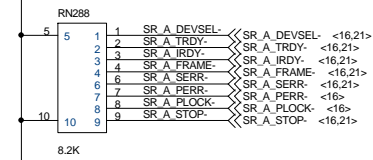
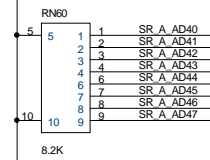
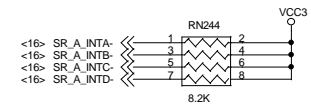
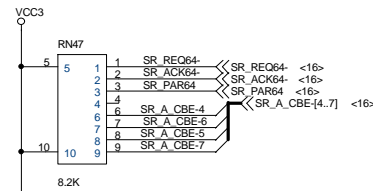
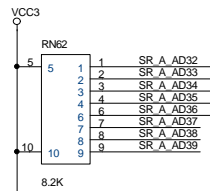
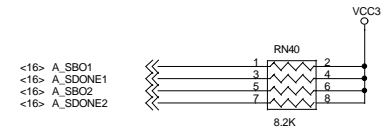
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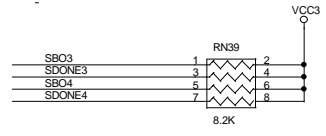
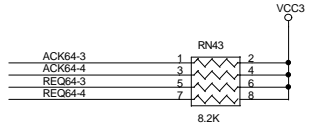
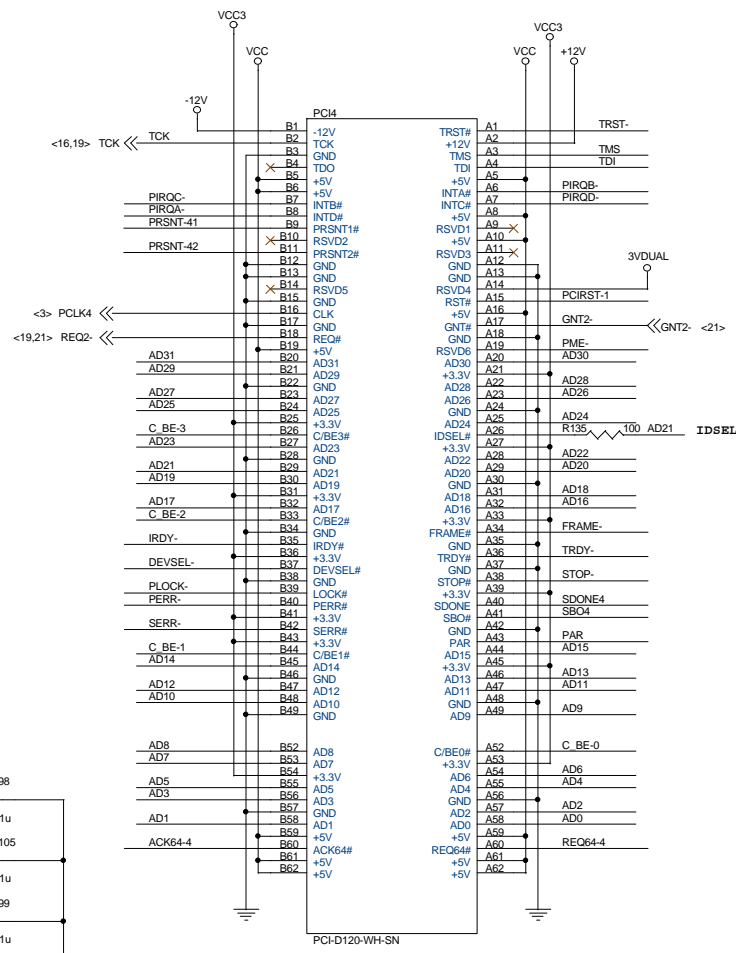
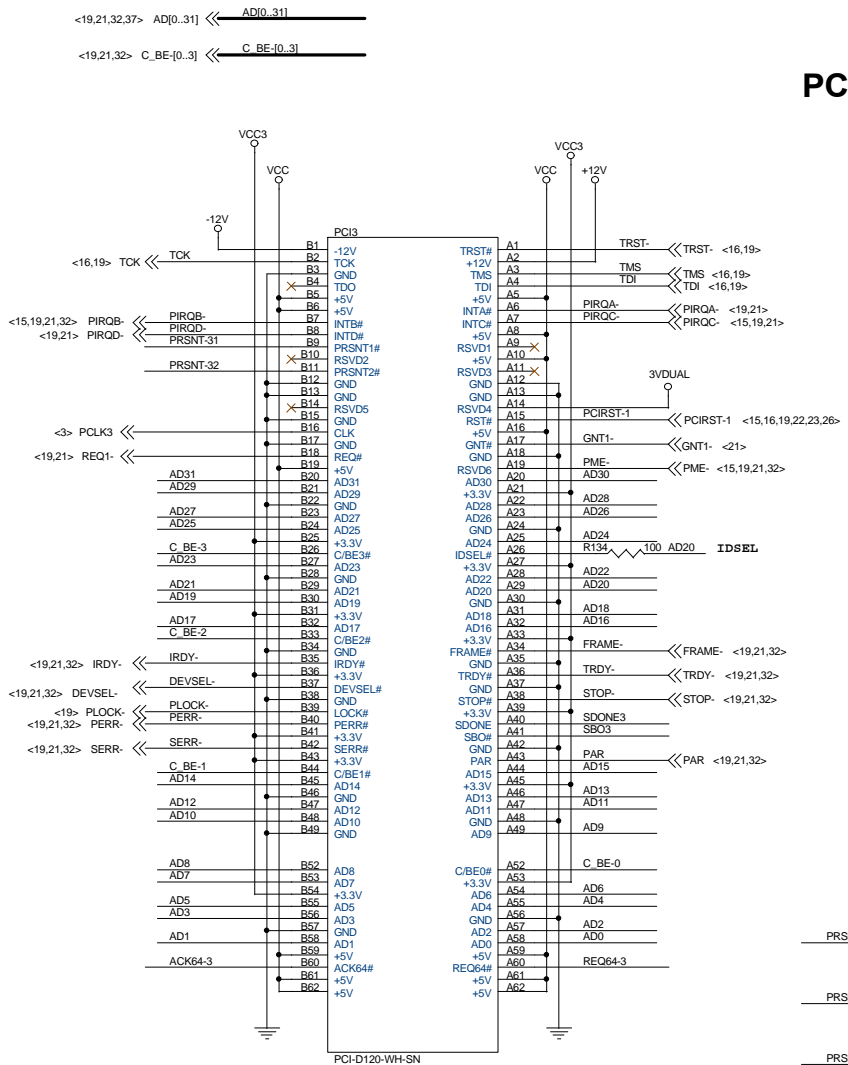
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RN232
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<11,16,36> A_PAR 8 1 SR_A_PAR <16,21>



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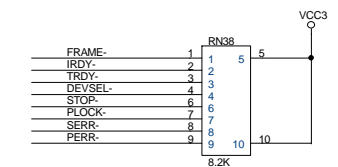
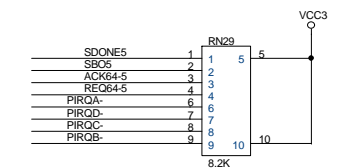
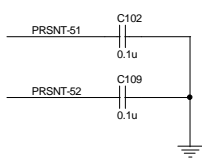
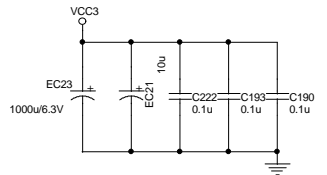
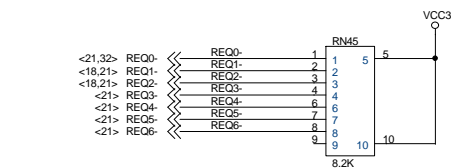
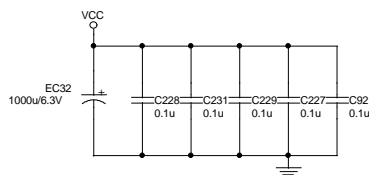
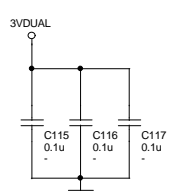
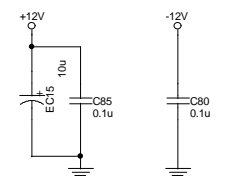
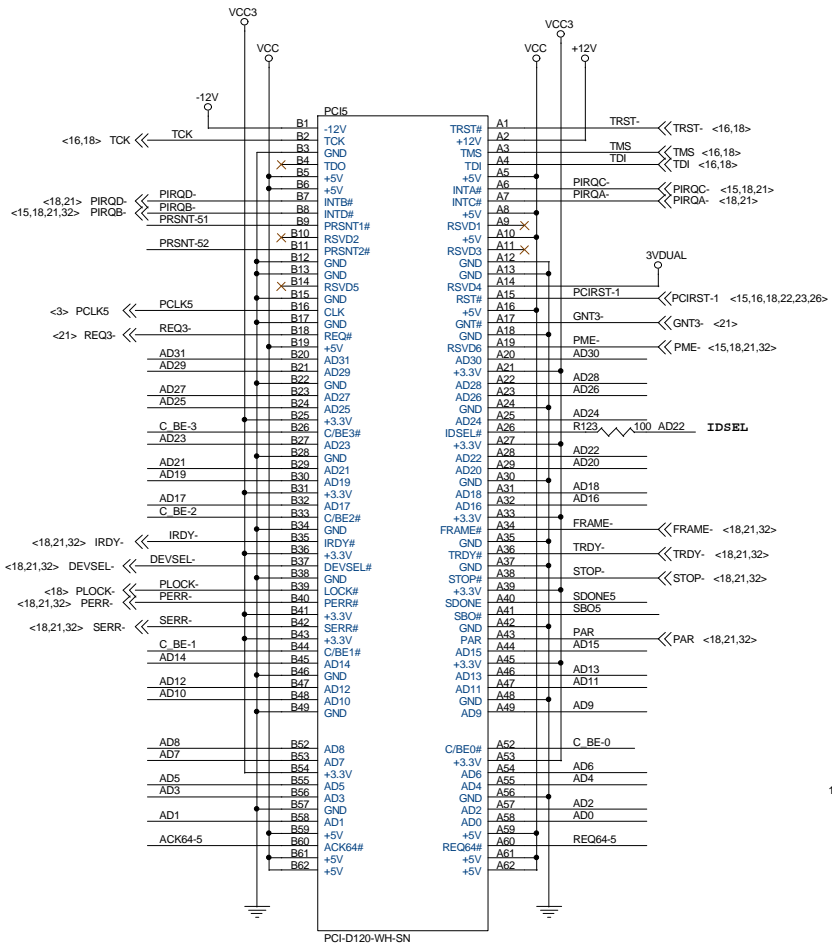
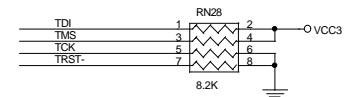
PCI Connector 3,4



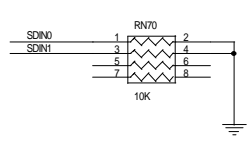
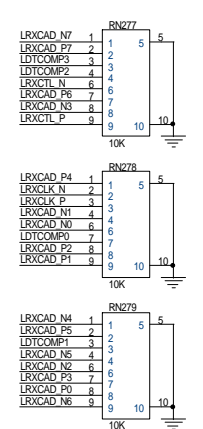
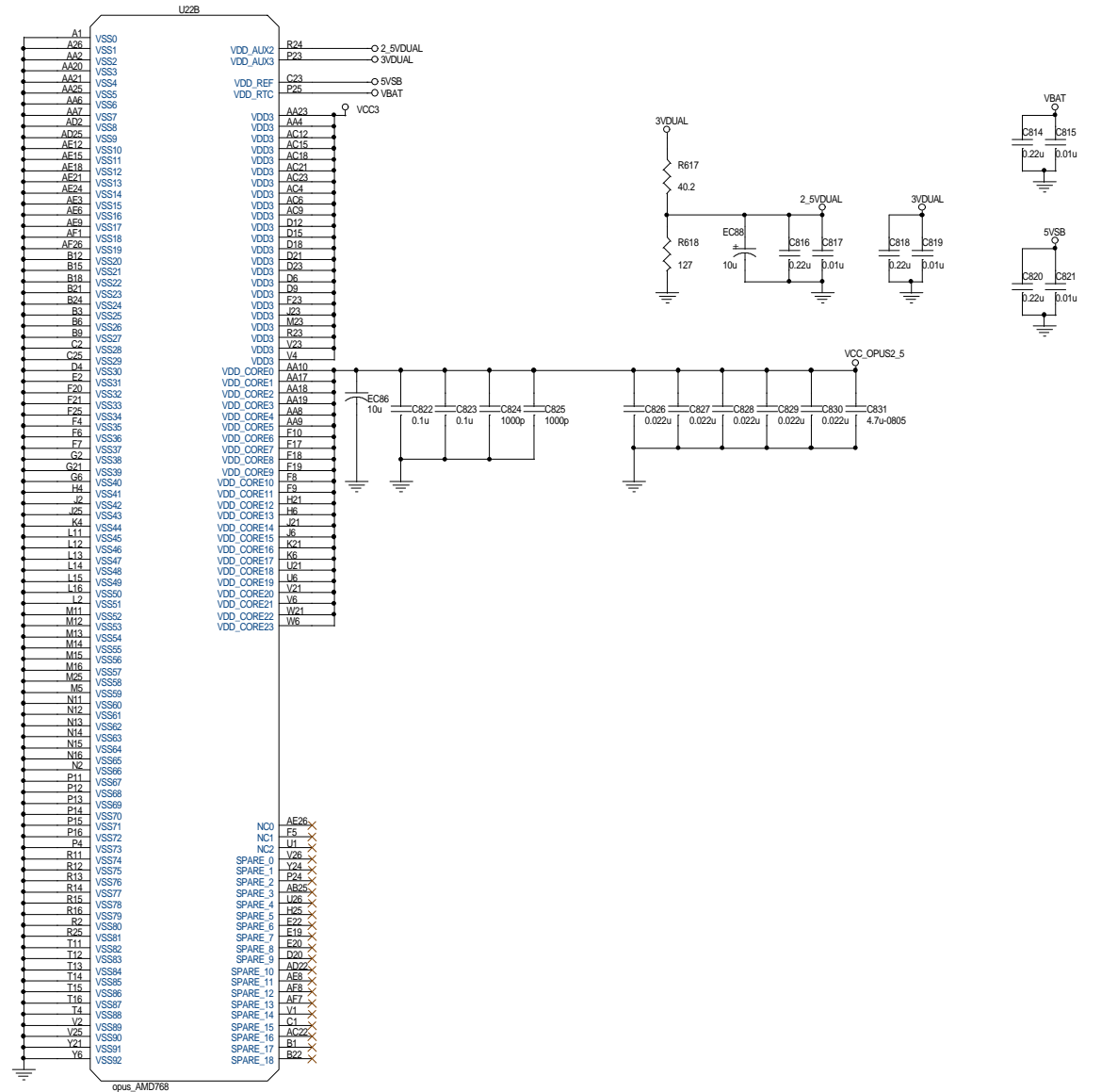
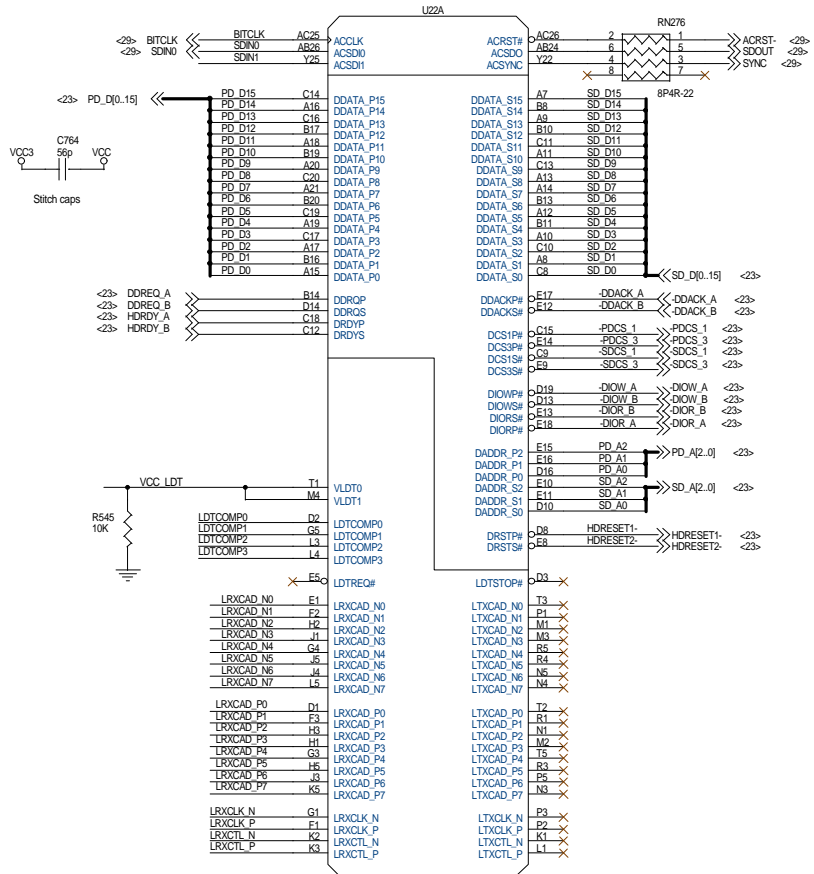
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Title PCI CONNECTOR 3,4		
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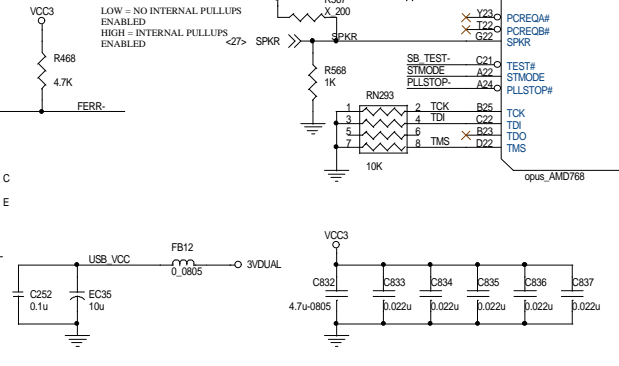
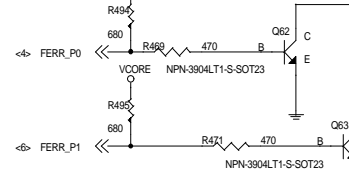
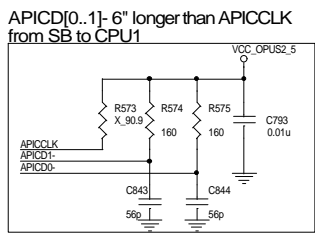
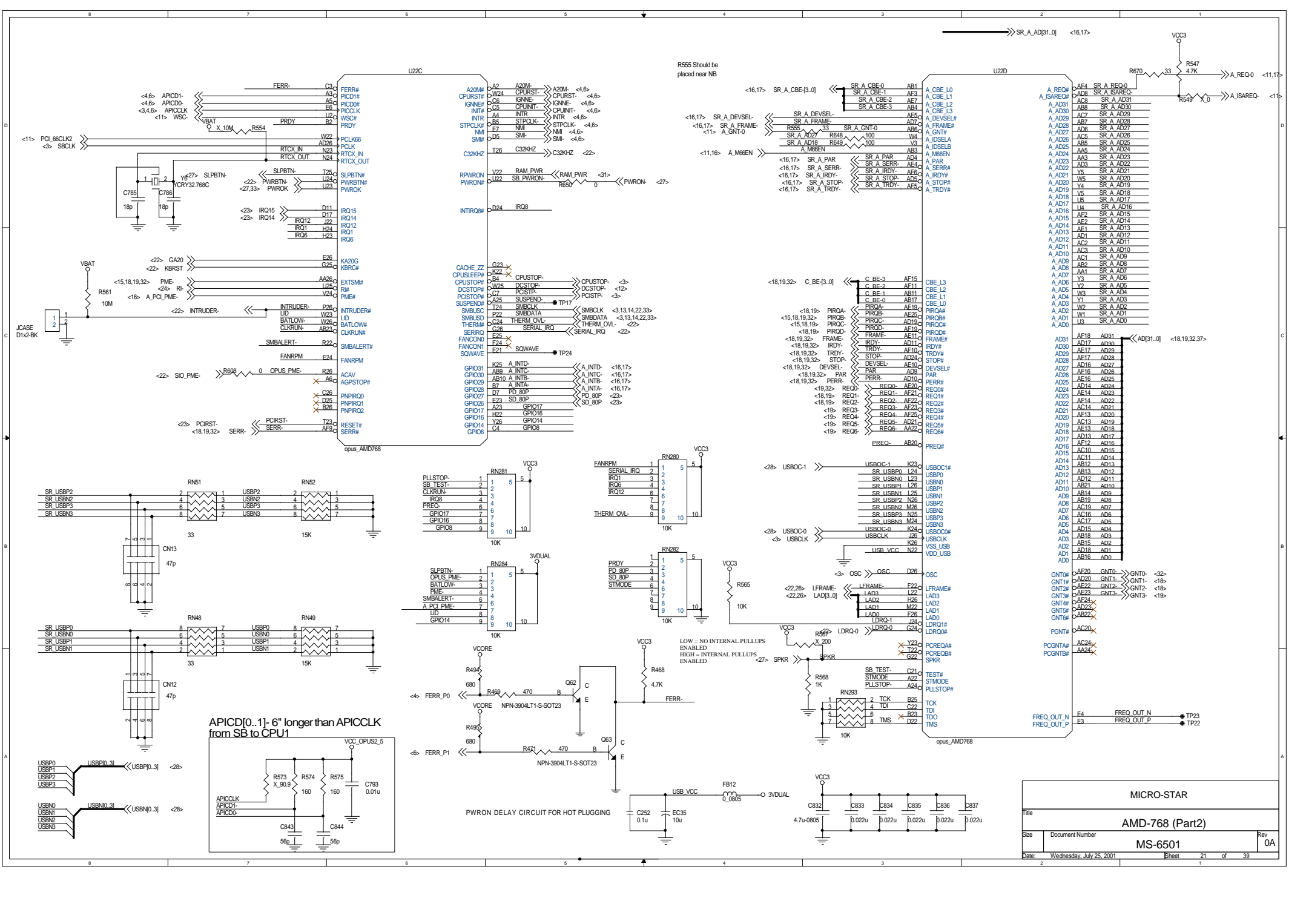
PCI Connector 5

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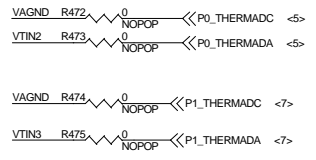
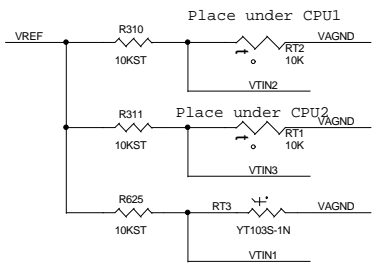


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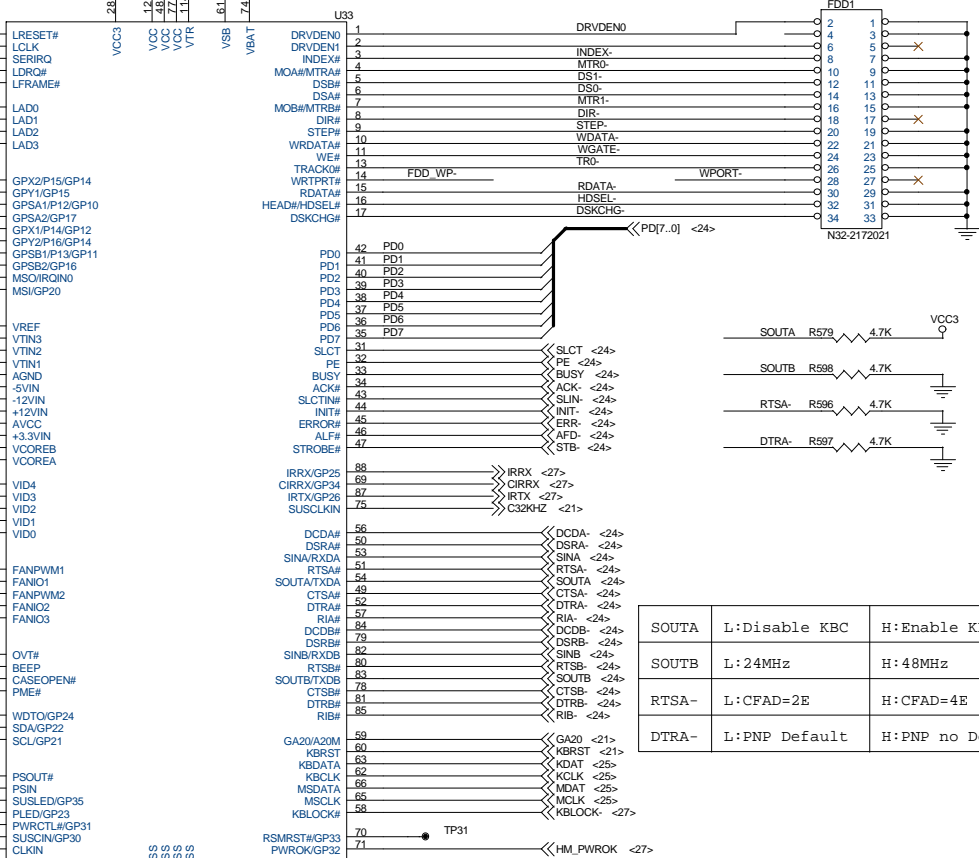
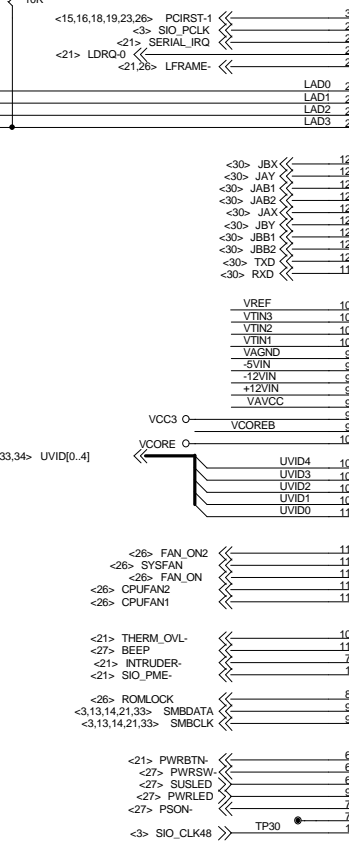
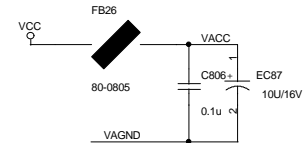
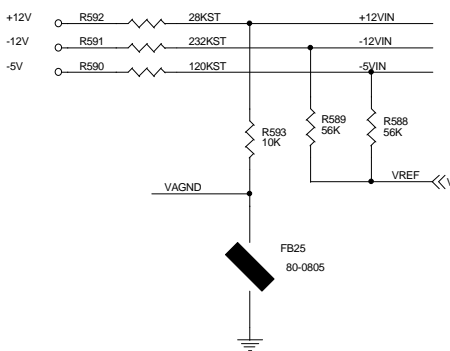
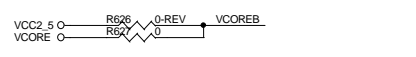
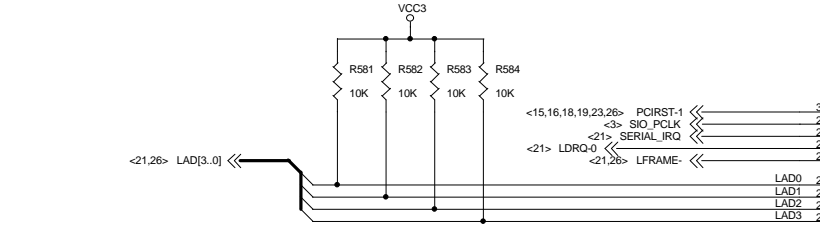
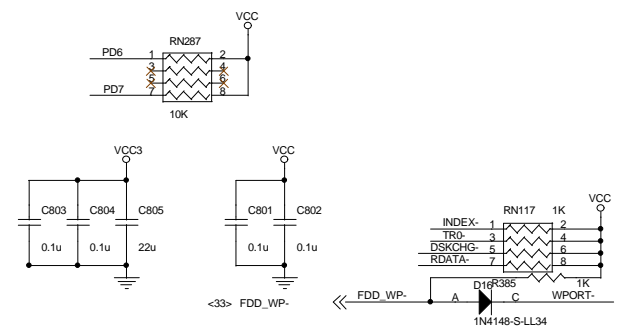


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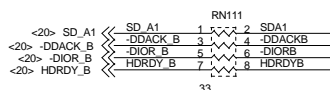
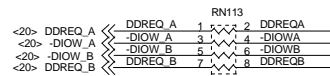
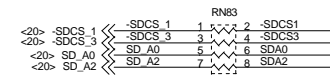
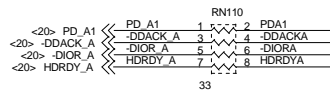
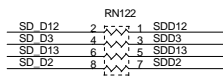
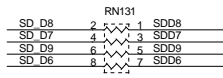
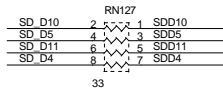
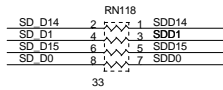
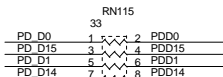
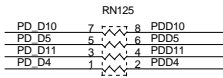
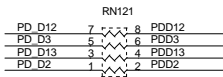
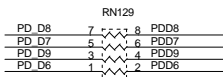
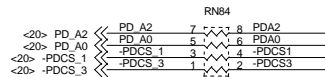
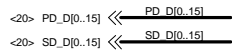


Place RT2 under CPU1

Place RT1 under CPU2

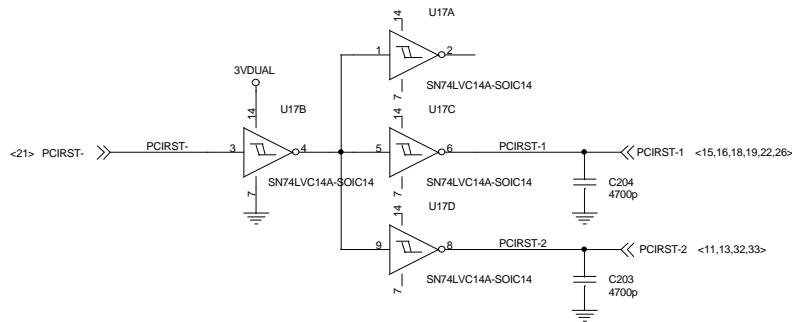
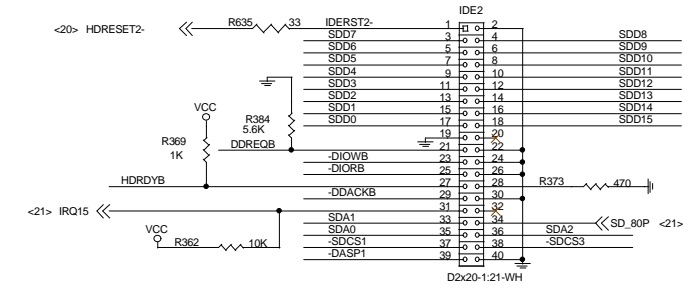
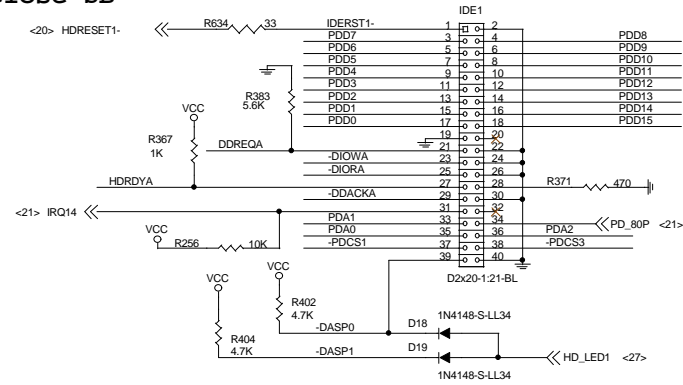


SOUTA	L:Disable KBC	H:Enable KBC
SOUTB	L:24MHz	H:48MHz
RTSA-	L:CFAD=2E	H:CFAD=4E
DTRA-	L:PNP Default	H:PNP no Default



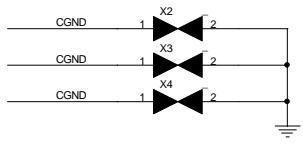
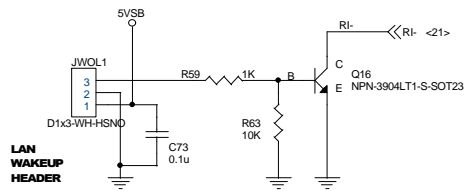
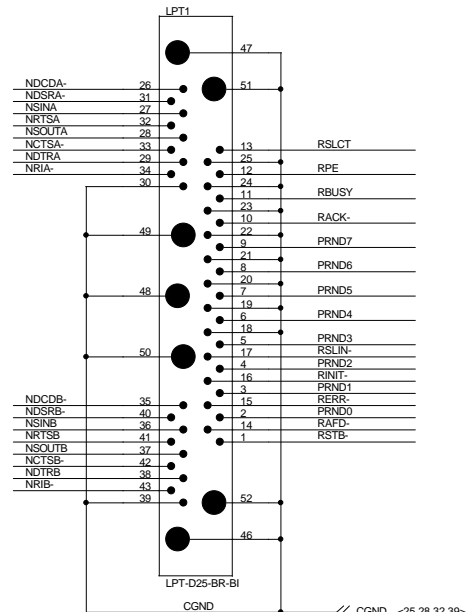
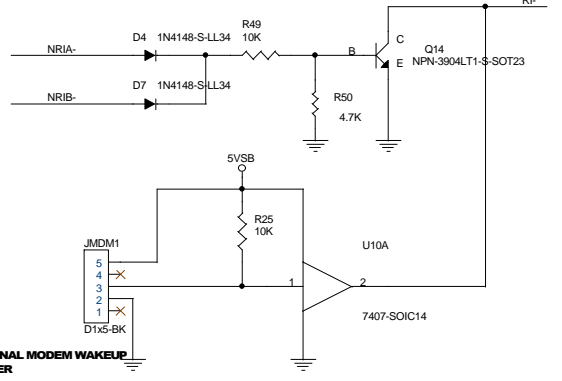
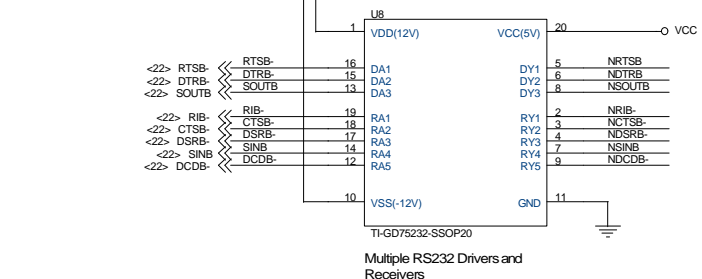
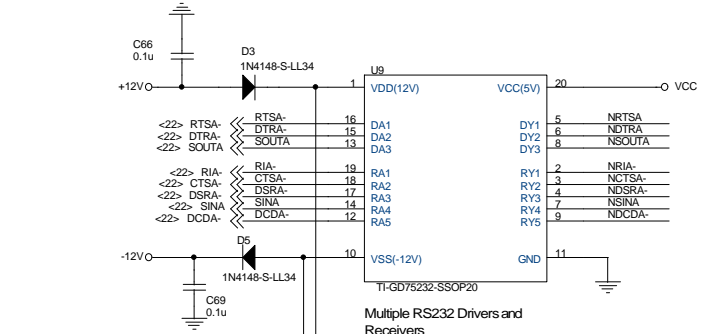
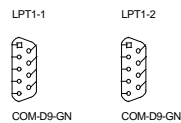
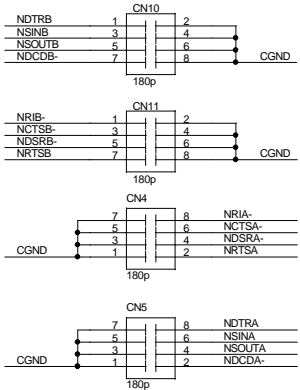
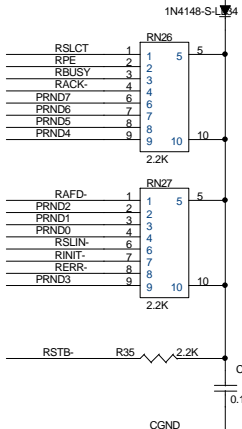
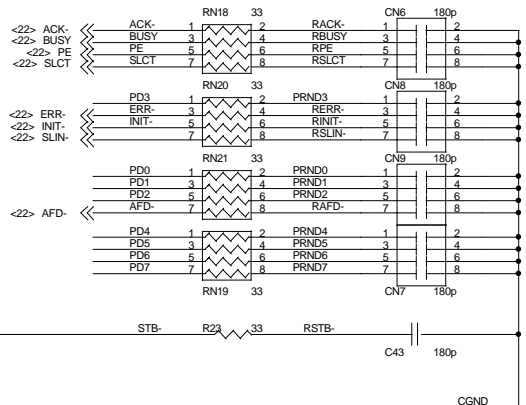
All series Res. should be very close SB

ATA33/66/100

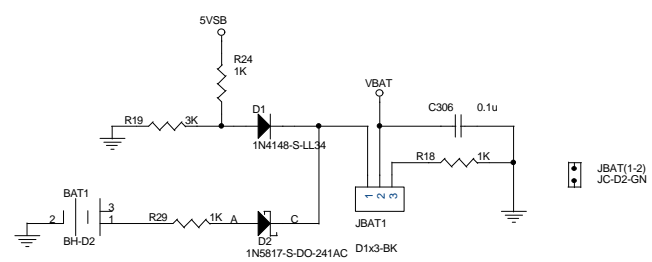
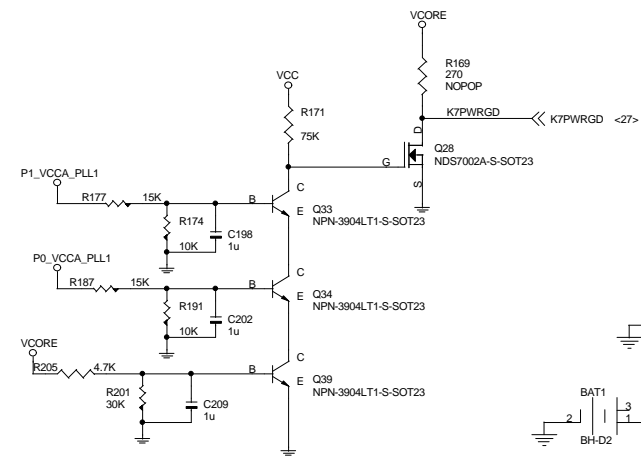
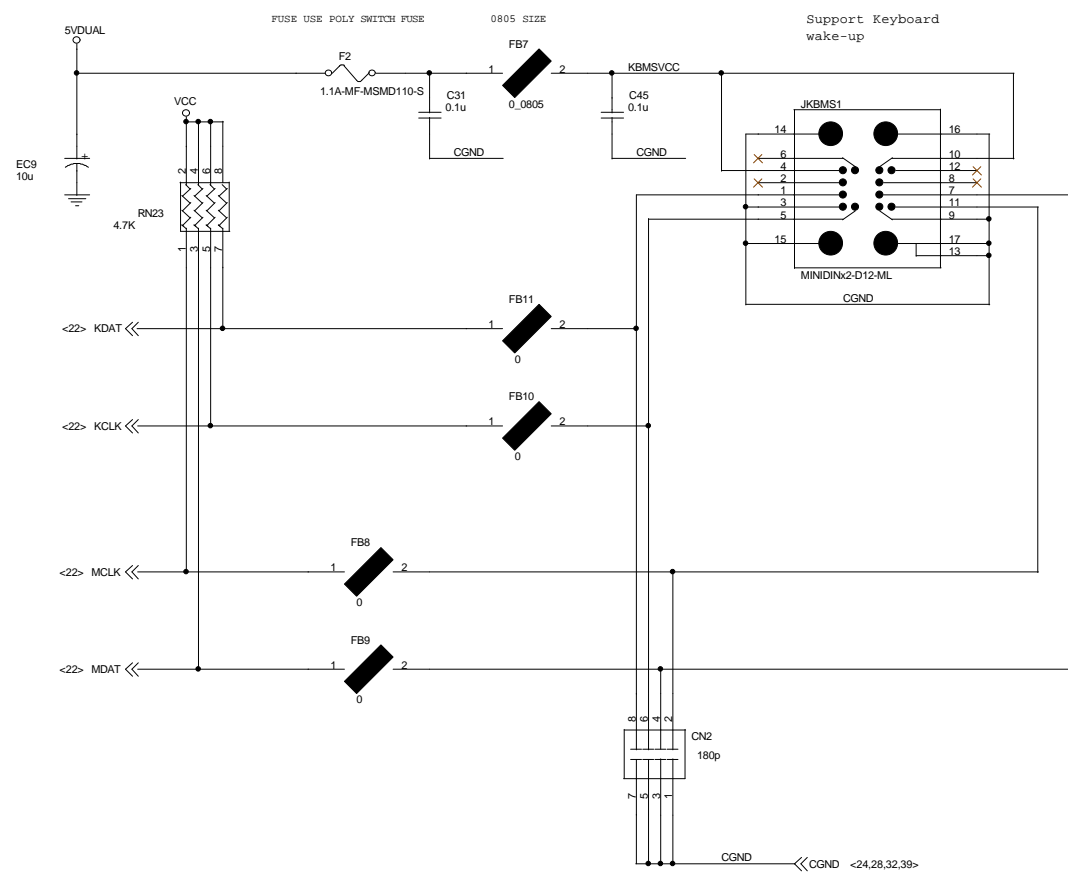


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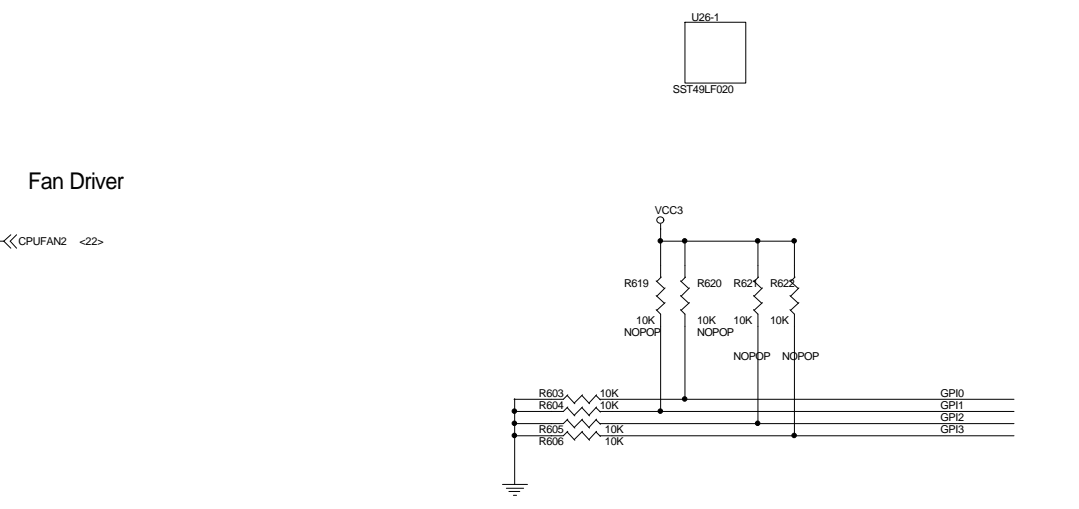
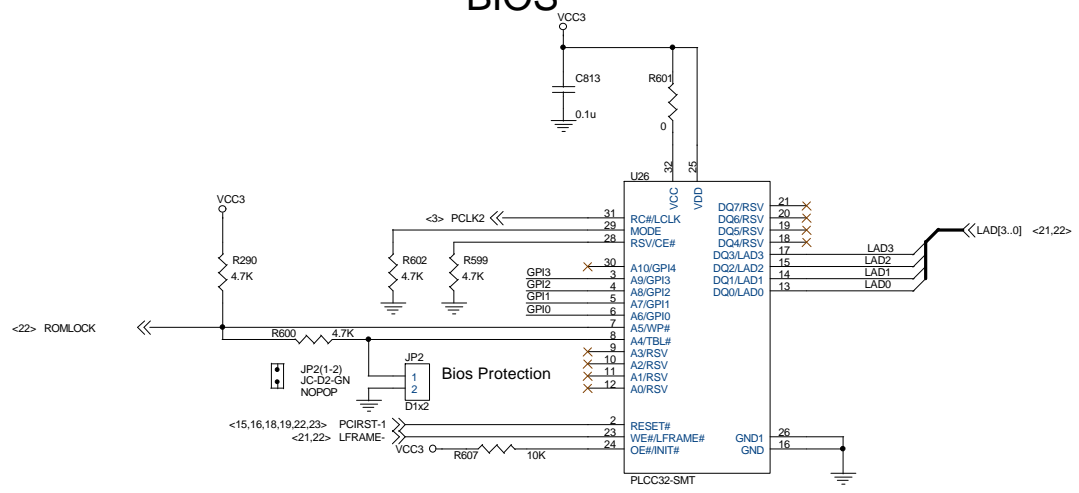


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LPT & COM Ports		
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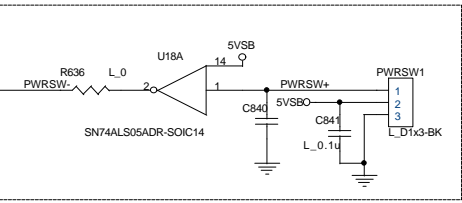
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BIOS

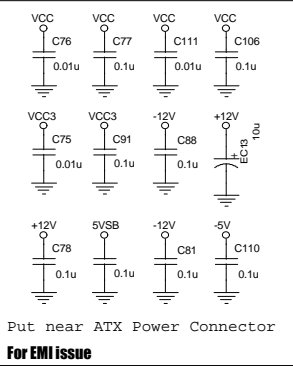
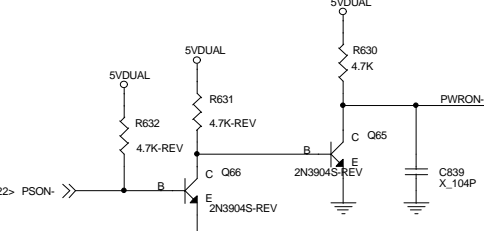
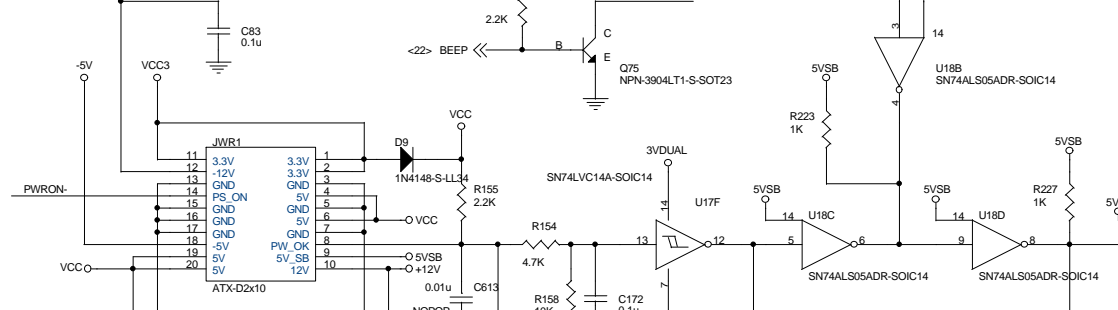
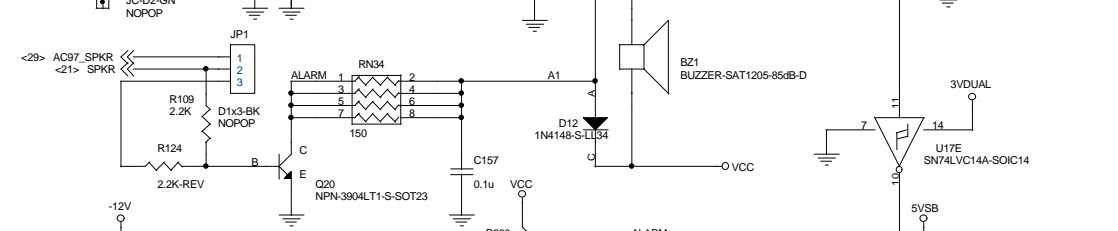
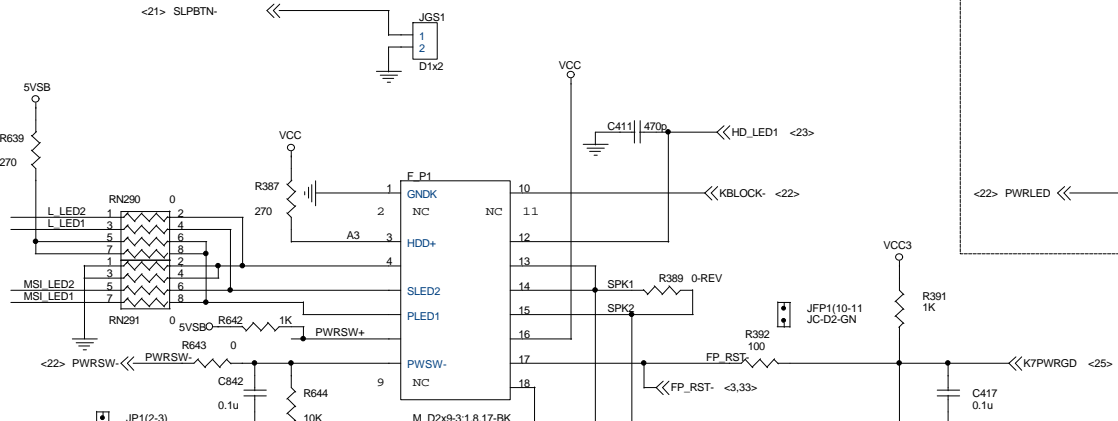
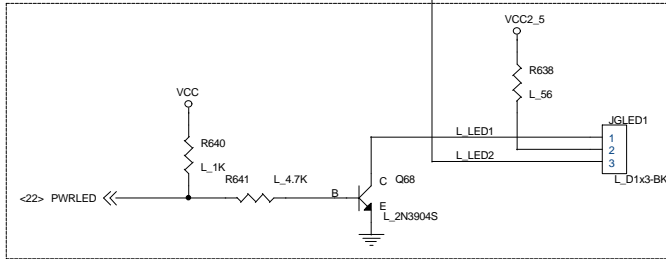
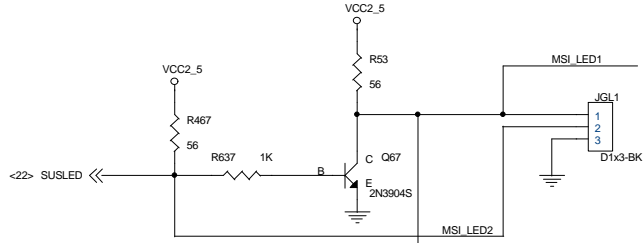
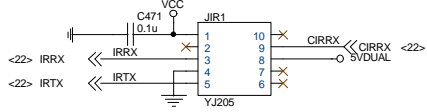


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BIOS & Fans			
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JP2(1-2)
JC-D2-GN
NOPOP



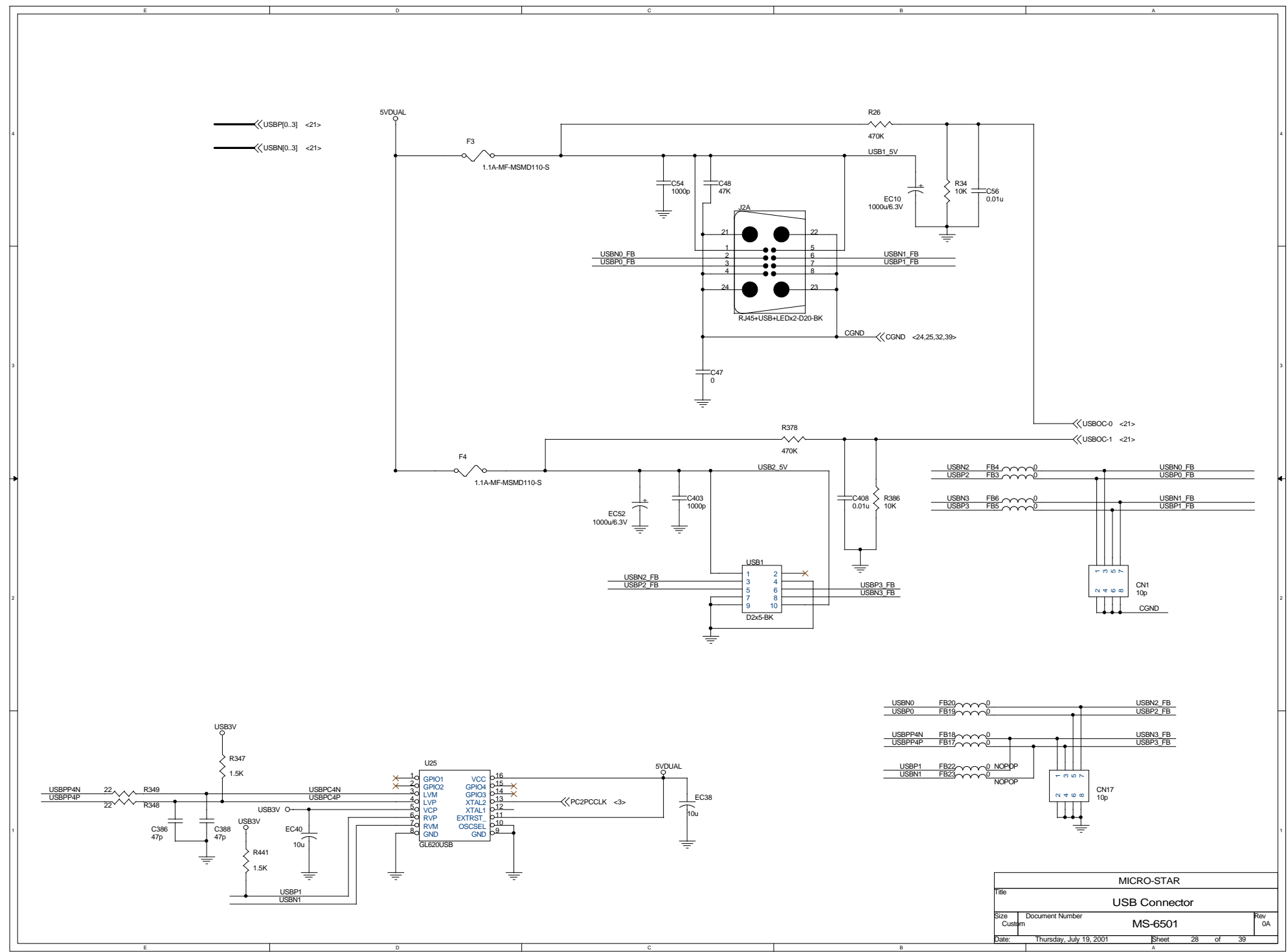
IR HEADER



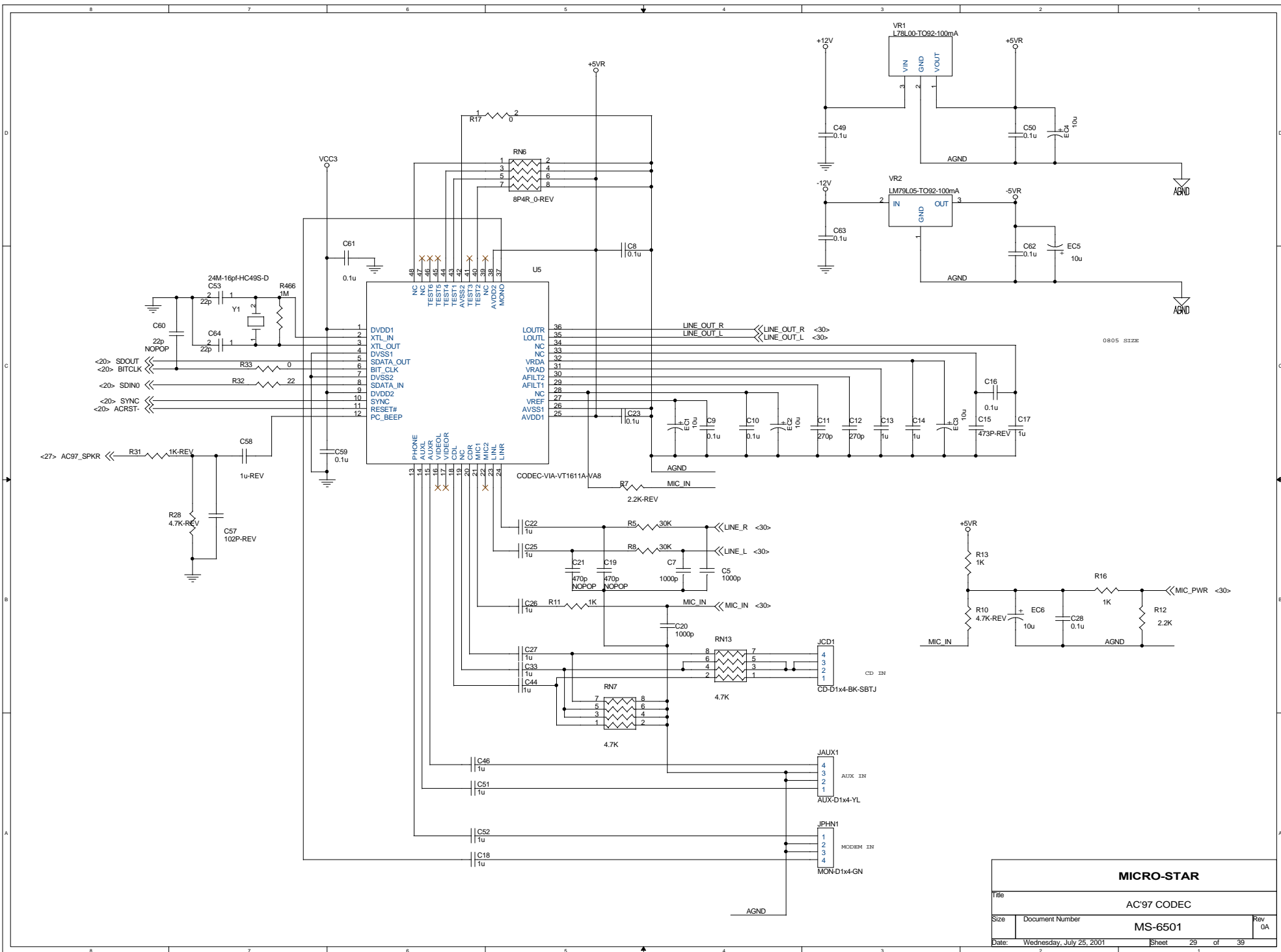
MICRO-STAR

Front Panel

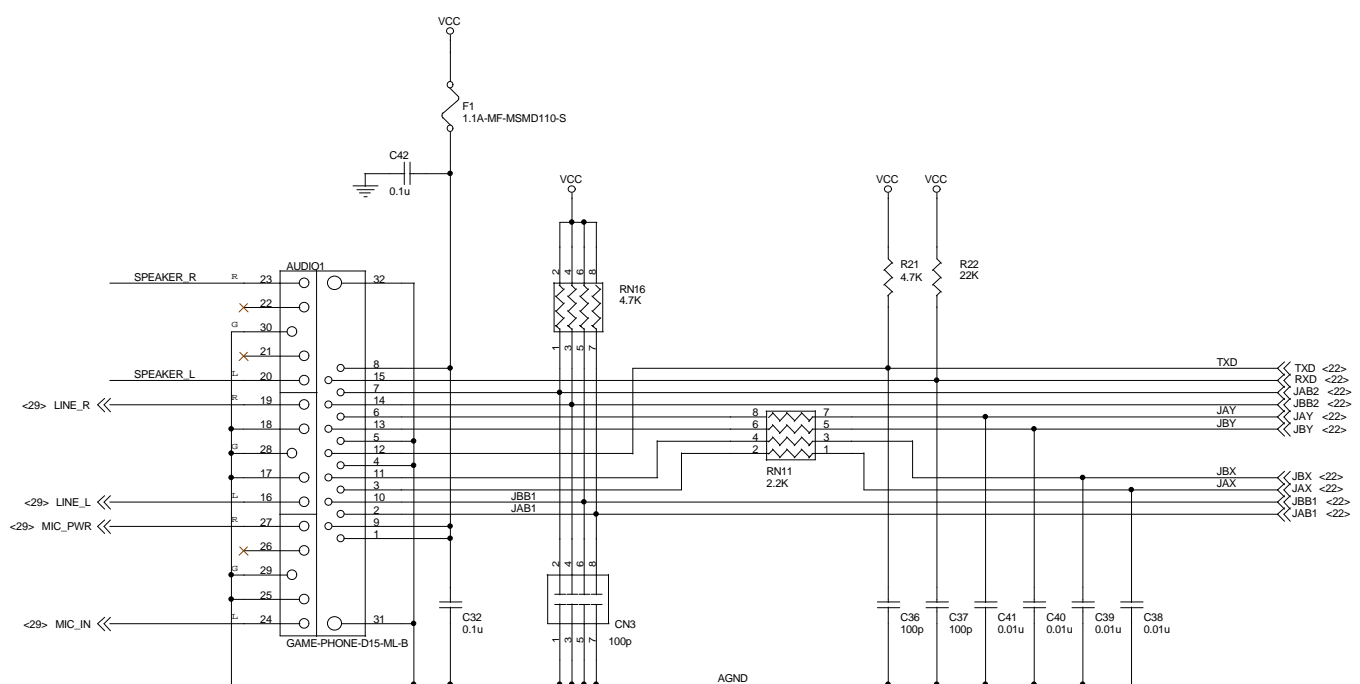
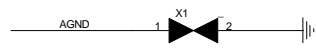
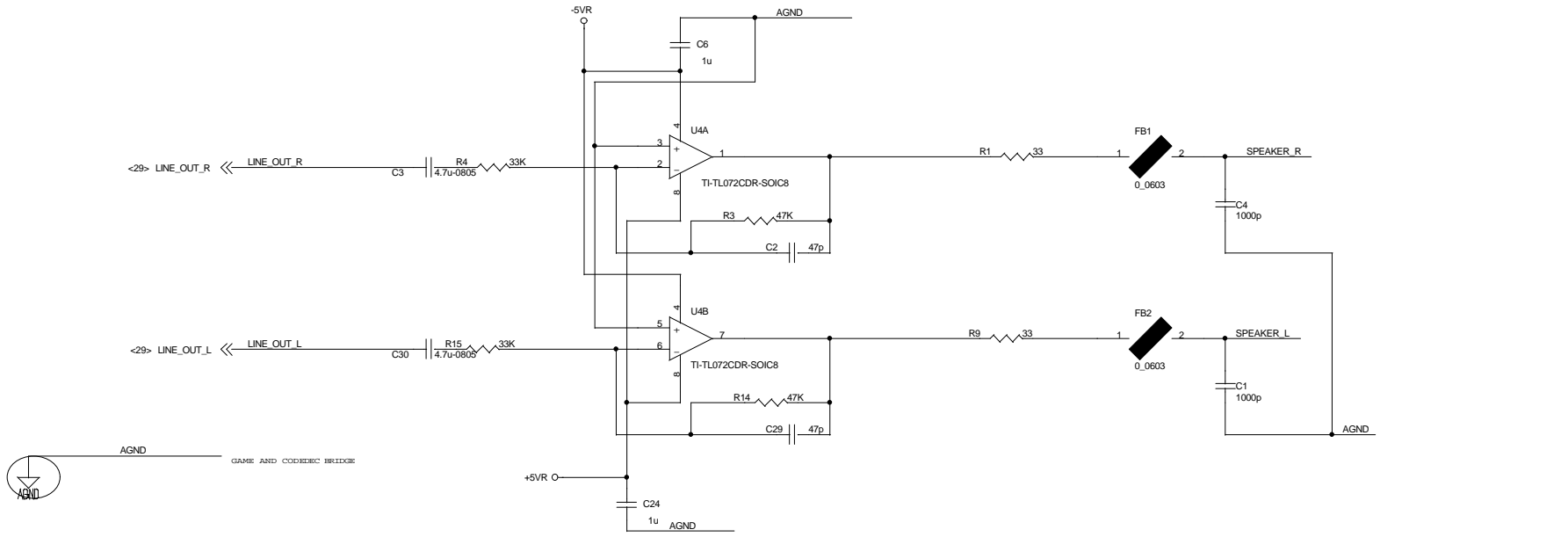
Title	Front Panel		Rev	0A
Size	Document Number	MS-6501		
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MICRO-STAR		
Title		
USB Connector		
Size	Document Number	Rev
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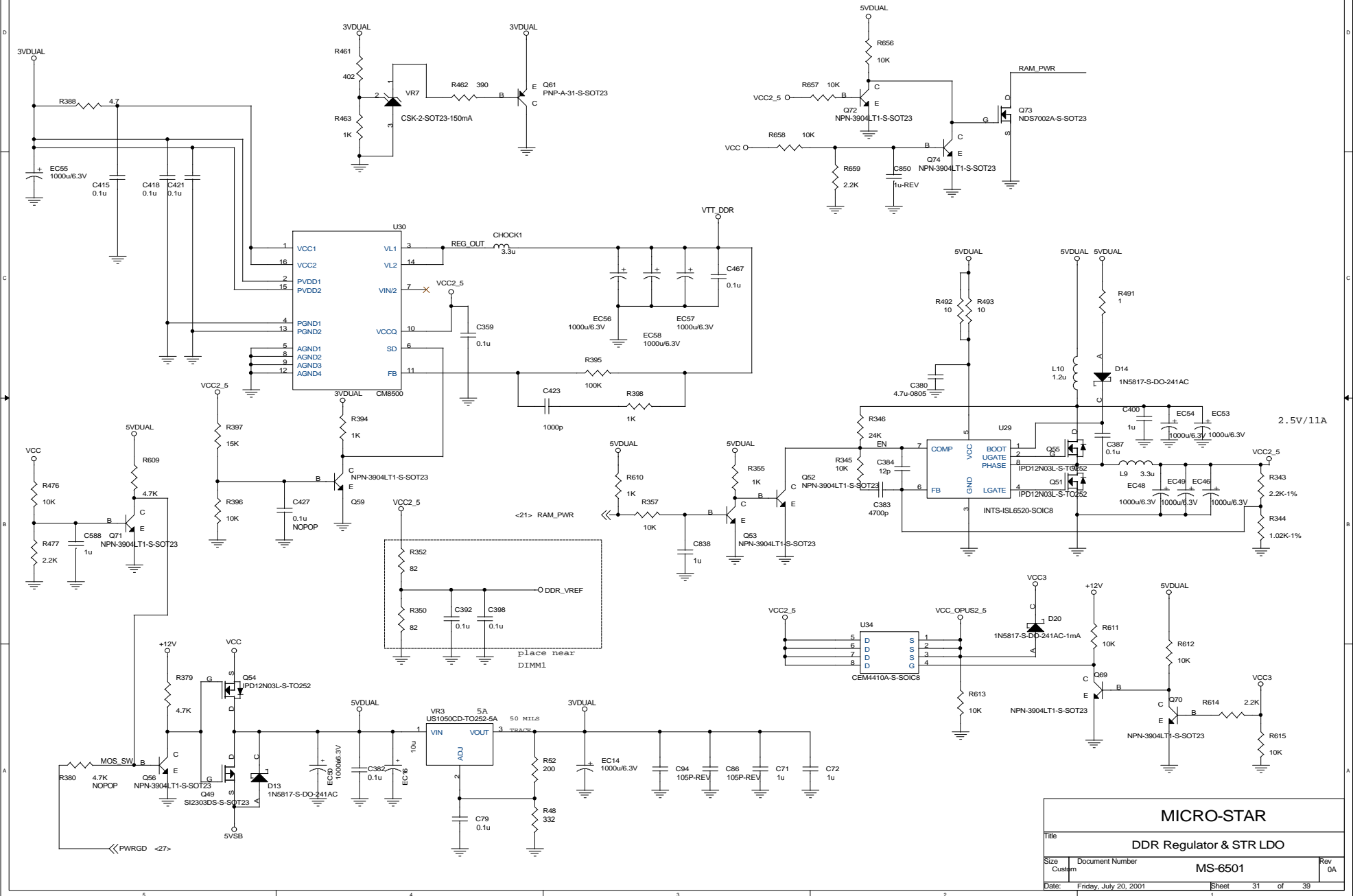


MICRO-STAR			
Title AC'97 CODEC			
Size	Document Number	Rev	0A
MS-6501			
Date: Wednesday, July 25, 2001	Sheet 29	of 39	

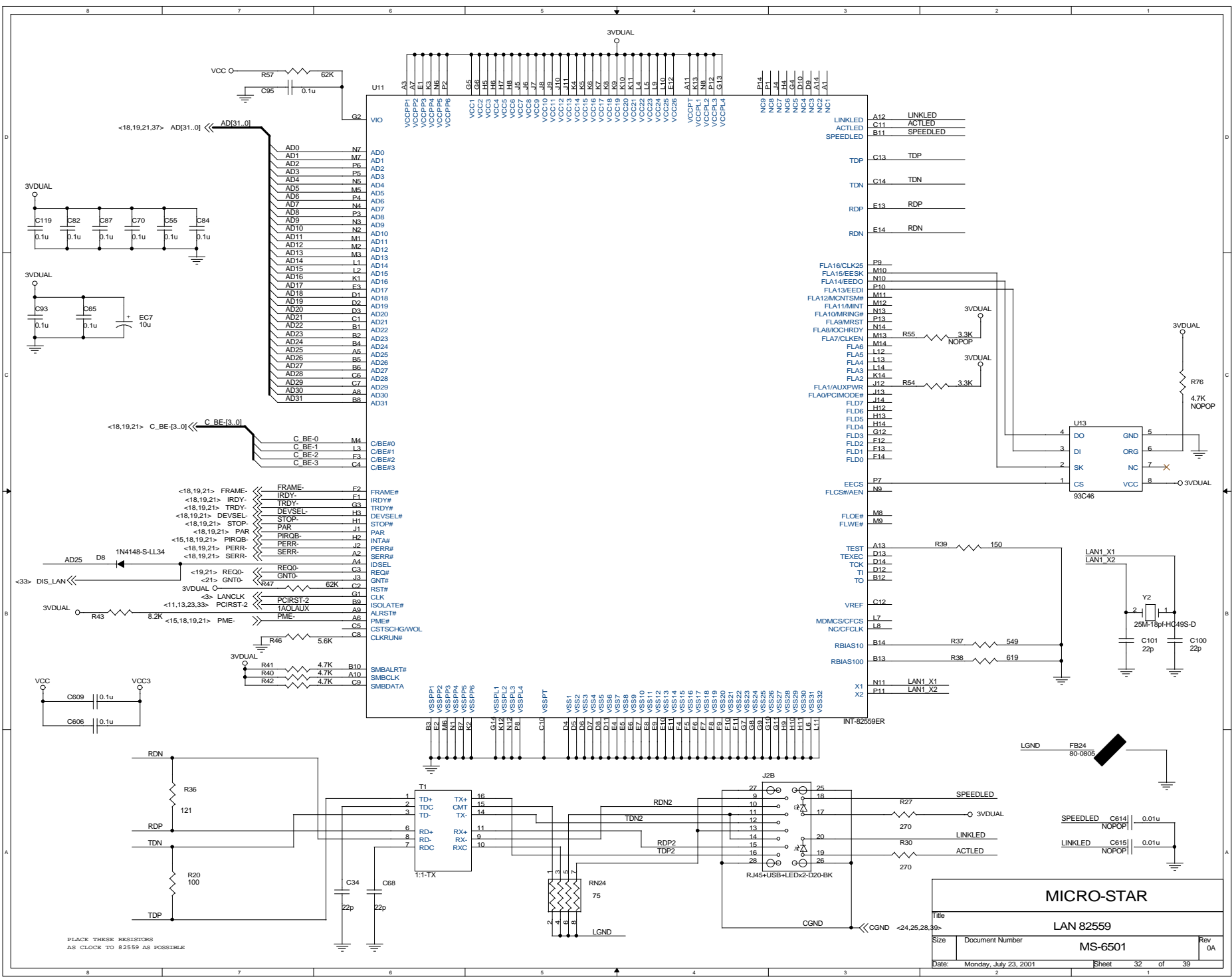


MICRO-STAR			
Title Audio/Game Port			
Size Custom	Document Number MS-6501	Rev 0A	
Date: Tuesday, July 24, 2001	Sheet 30	of 39	

DDR Regulator & STR LDO

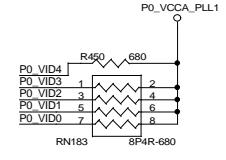
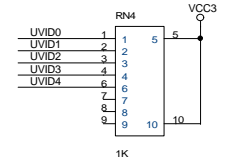
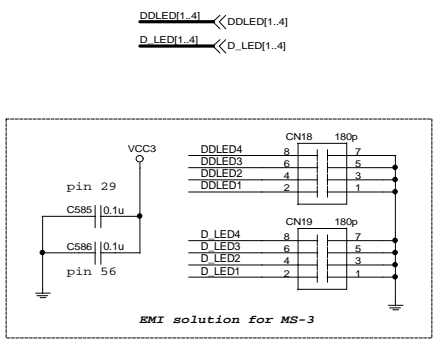
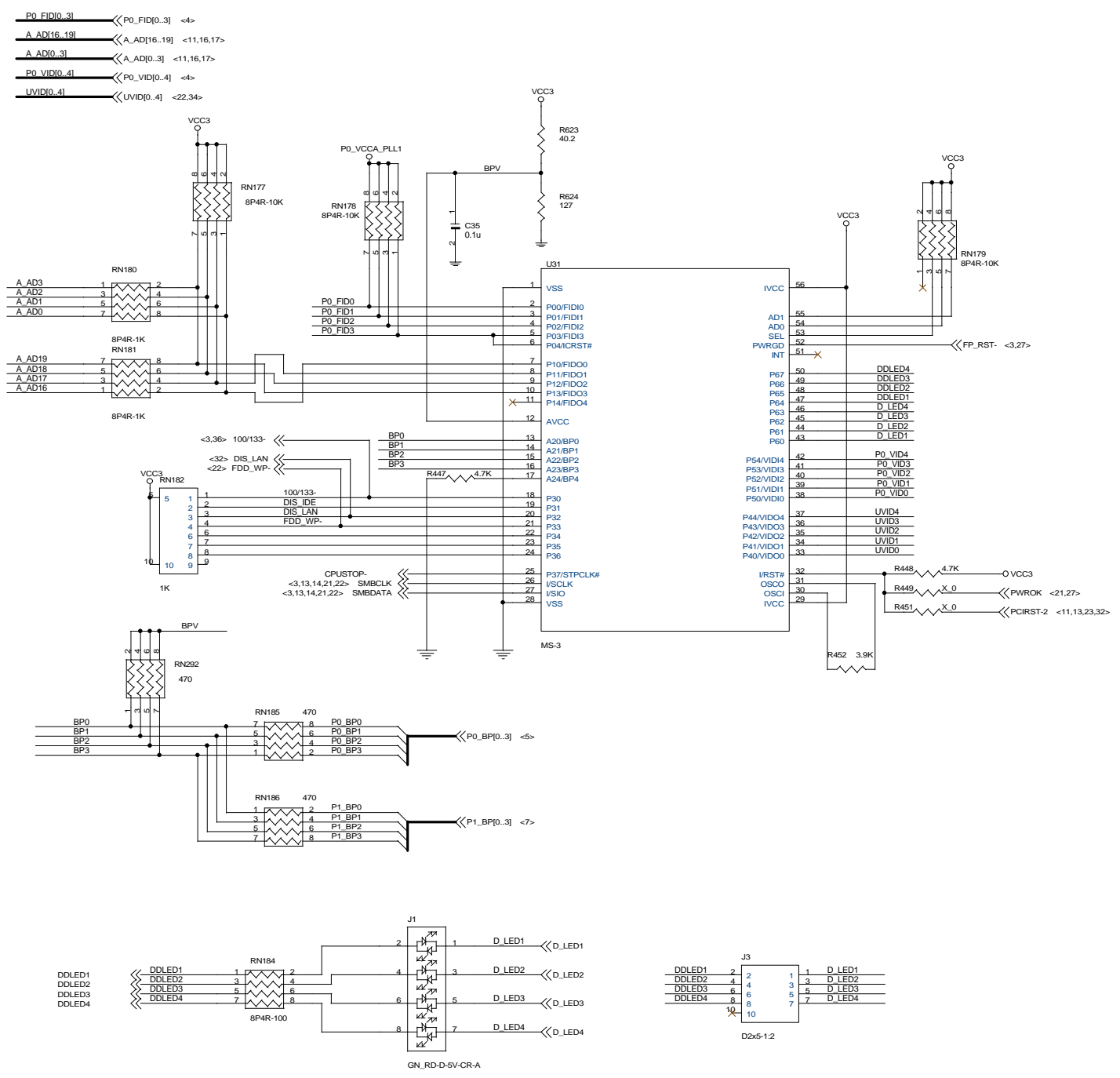


MICRO-STAR			
Title DDR Regulator & STR LDO			
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LAN 82559		
Title	LAN 82559	
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PLACE THESE RESISTORS AS CLOSE TO 82559 AS POSSIBLE

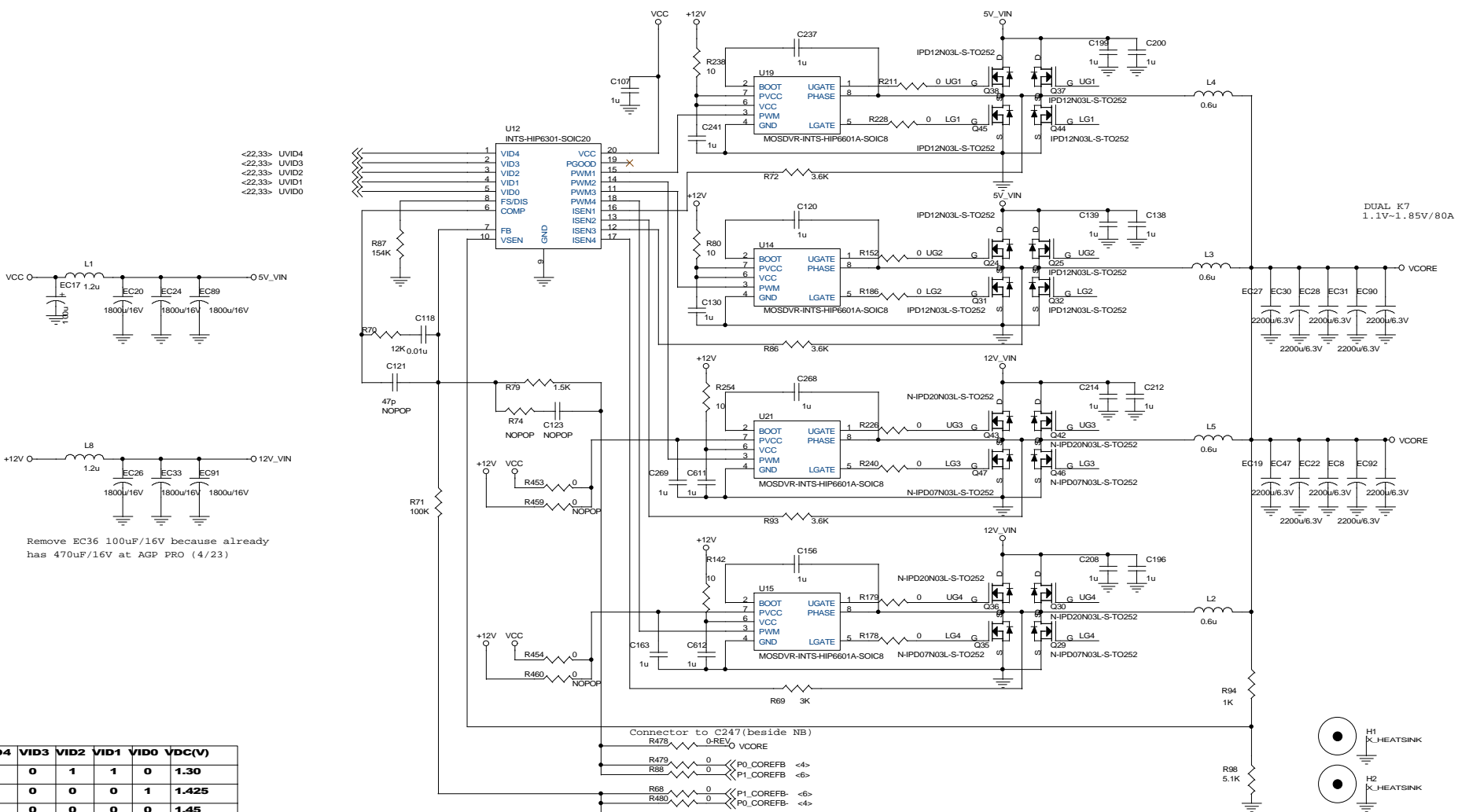


* 25 mils Trace/ 12 mils Space

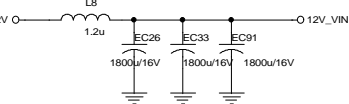
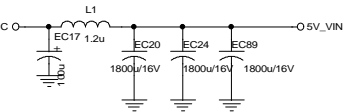
MICRO-STAR		
Title		
MS-6501		
Size Custom	Document Number	Rev 0A
VCORE AJUST		
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Voltage Regular Module

All N-Channel MOSFET use TO-252



<22.33> UVID4
 <22.33> UVID3
 <22.33> UVID2
 <22.33> UVID1
 <22.33> UVID0

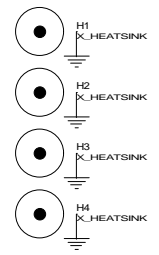
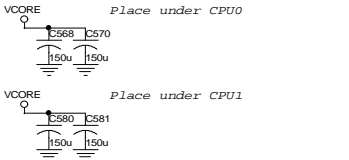
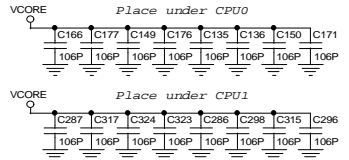


Remove EC36 100uF/16V because already has 470uF/16V at AGP PRO (4/23)

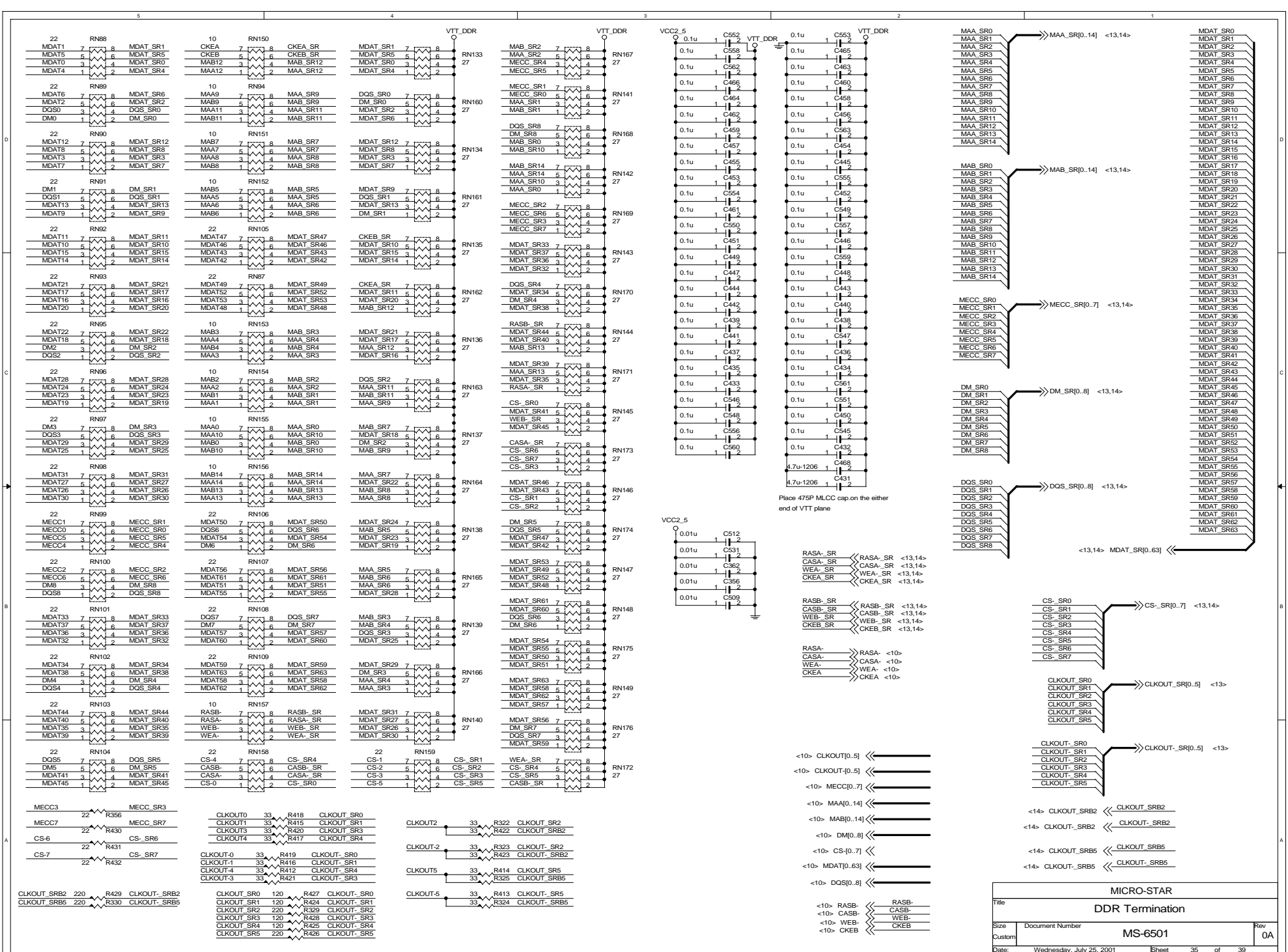
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	0	1	1	1	1.675
0	0	1	1	0	1.700

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

Design for 45A @ +/- 100 mV



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MS-6501		
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MICRO-STAR			
DDR Termination			
File	Document Number		Rev
Size	MS-6501		0A
Custom			
Date:	Wednesday, July 25, 2001		Sheet 35 of 39

A_AD[11:10] CPU0 Physical S2K Bus Length

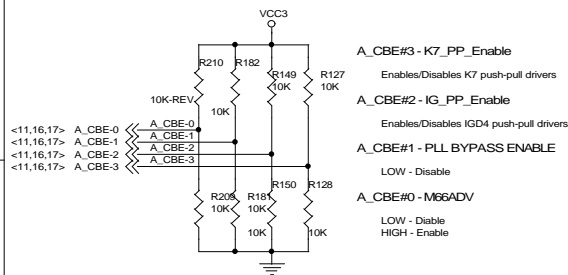
- 00 - Short non-slotA
- 01 - Single Slot A or "close"
- 10 - Far dual Slot A
- 11 - Farthest possible Slot A

A_AD[27:26] CPU1 Physical S2K Bus Length AD[27:26]

- 00 - Short non-slotA
- 01 - Single Slot A or "close"
- 10 - Far dual Slot A
- 11 - Farthest possible Slot A

A_AD[15] 66MHz PCI

- LOW -> Disable 66MHz PCI Mode
- HIGH -> Enable 66MHz PCI Mode



A_CBE#3 - K7_PP_Enable

Enables/Disables K7 push-pull drivers

A_CBE#2 - IG_PP_Enable

Enables/Disables IGD4 push-pull drivers

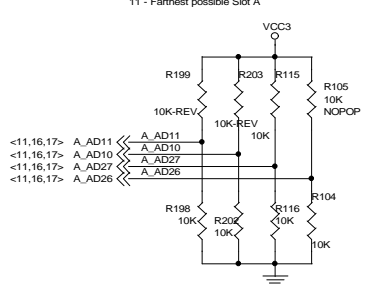
A_CBE#1 - PLL BYPASS ENABLE

LOW - Disable

A_CBE#0 - M66ADV

LOW - Disable

HIGH - Enable



A_AD[14:12] AGP Clock Mux[2:0]

A_AD[9] Bypass_PLLs

A_AD[8] Outclk_Delay_Enable

Enables PLL bypass mode when TEST# is asserted.

A_AD[7:5] SysClock_Mux[2:0]

Enables K7 OUTCLK delay. Default is disabled.

A_AD[4] IGD4 Threshold Range Select for S2k Cells is

Selects input APLL clock mux for PLL test mode. Refer to Ch. 11 of IGD4 Differences Document

Selects input SPLL clock mux for PLL test mode. Refer to Ch. 11 of IGD4 Differences Document

Low - Threshold sense set to between 0.6V and 1.0V.

High - S2k Threshold sense set to between 1.0V and 1.4V.

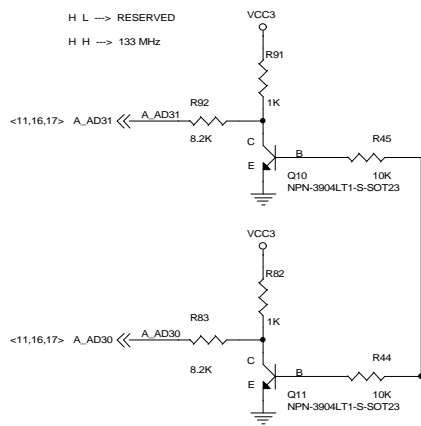
A_AD[31:30] CLK SPEED

L L -> 100 Mhz (DEFAULT)

L H -> 66 Mhz

H L -> RESERVED

H H -> 133 Mhz



A_AD[25] TRISTATE_ENABLE

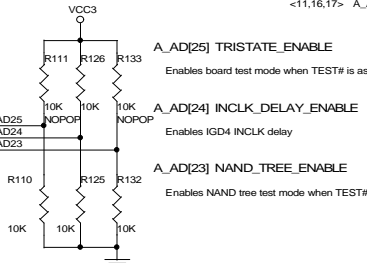
Enables board test mode when TEST# is asserted

A_AD[24] INCLK_DELAY_ENABLE

Enables IGD4 INCLK delay

A_AD[23] NAND_TREE_ENABLE

Enables NAND tree test mode when TEST# is asserted



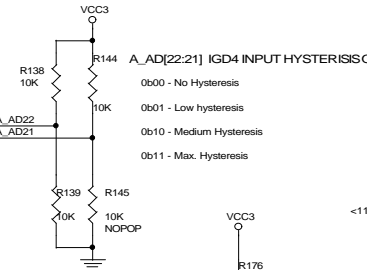
A_AD[22:21] IGD4 INPUT HYSTERESIS OF OUTCLKs

0b00 - No Hysteresis

0b01 - Low hysteresis

0b10 - Medium Hysteresis

0b11 - Max. Hysteresis



A_AD[29] Disable Divider

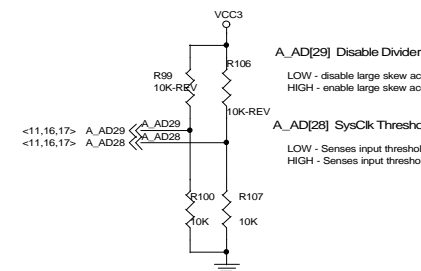
LOW - disable large skew accommodation mode

HIGH - enable large skew accommodation mode

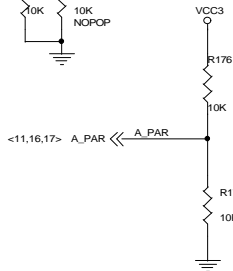
A_AD[28] SysClk Threshold

LOW - Senses input thresholds between 0.6V and 1.0V.

HIGH - Senses input thresholds between 1.0V and 1.4V.



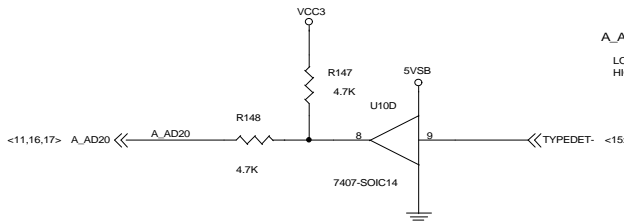
A pullup on A_PAR will put IGD4 into clock test mode when TEST# is low



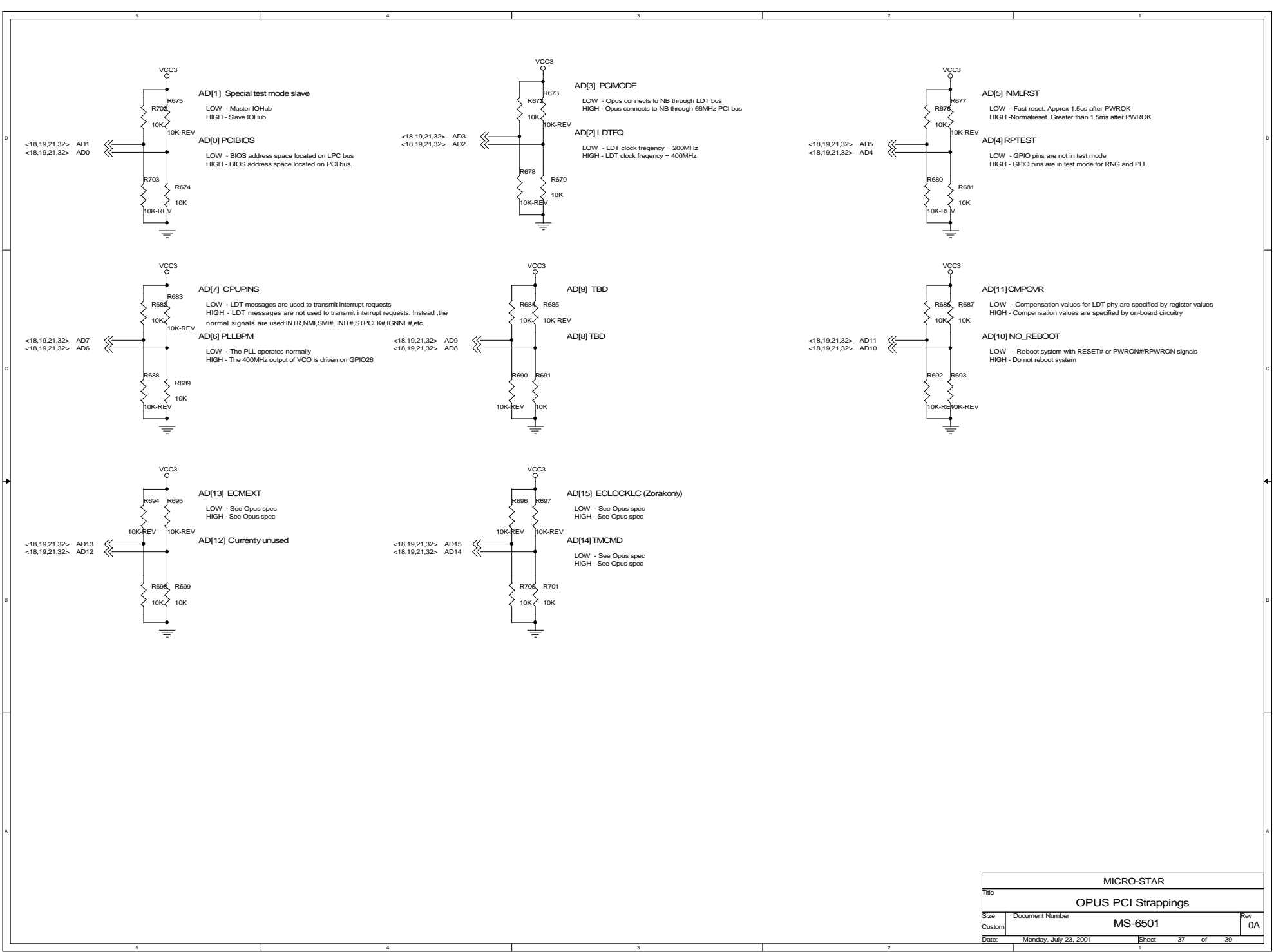
A_AD[20] AGP TYPEDET

LOW - AGP Card with VDD_AGP = 1.5V installed

HIGH - AGP Card with VDD_AGP = 3.3V installed



MICRO-STAR		
Title IGD4 PCI Strappings		
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AD[1] Special test mode slave

LOW - Master IOHub
HIGH - Slave IOHub

AD[0] PCIBIOS

LOW - BIOS address space located on LPC bus
HIGH - BIOS address space located on PCI bus.

AD[3] PCIMODE

LOW - Opus connects to NB through LDT bus
HIGH - Opus connects to NB through 66MHz PCI bus

AD[2] LDTFQ

LOW - LDT clock frequency = 200MHz
HIGH - LDT clock frequency = 400MHz

AD[5] NMLRST

LOW - Fast reset. Approx 1.5us after PWROK
HIGH - Normalreset. Greater than 1.5ms after PWROK

AD[4] RPTEST

LOW - GPIO pins are not in test mode
HIGH - GPIO pins are in test mode for RNG and PLL

AD[7] CPUPINS

LOW - LDT messages are used to transmit interrupt requests
HIGH - LDT messages are not used to transmit interrupt requests. Instead, the normal signals are used: INTR, NMI, SMIF#, INIT#, STPCLK#, IGNNE#, etc.

AD[6] PLLBPM

LOW - The PLL operates normally
HIGH - The 400MHz output of VCO is driven on GPIO26

AD[9] TBD

AD[8] TBD

AD[11] CMPOVR

LOW - Compensation values for LDT phy are specified by register values
HIGH - Compensation values are specified by on-board circuitry

AD[10] NO_REBOOT

LOW - Reboot system with RESET# or PWRON#/RPWRON signals
HIGH - Do not reboot system

AD[13] ECMEXT

LOW - See Opus spec
HIGH - See Opus spec

AD[12] Currently unused

AD[15] ECLOCKLC (Zorakonly)

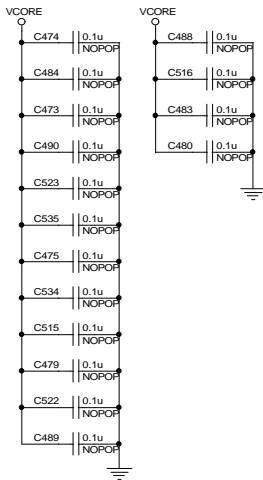
LOW - See Opus spec
HIGH - See Opus spec

AD[14] TMCMD

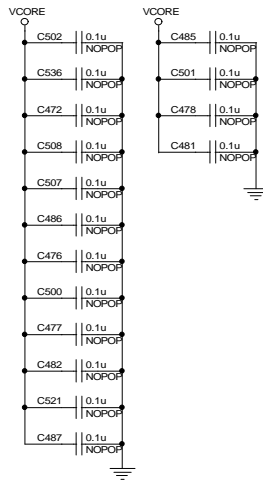
LOW - See Opus spec
HIGH - See Opus spec

MICRO-STAR			
Title OPUS PCI Strappings			
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Place at solder side of CPU0

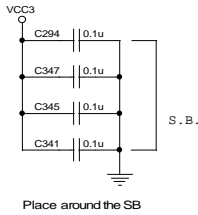
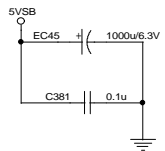
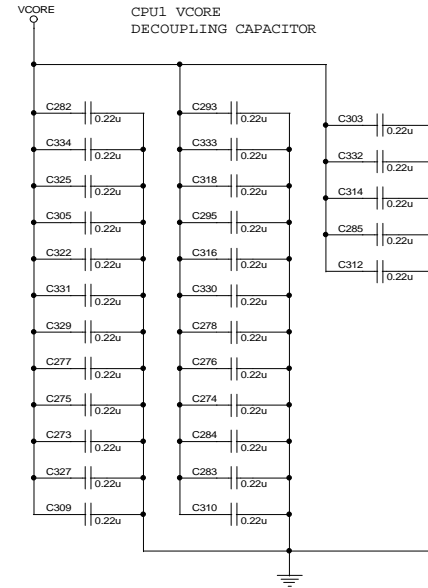
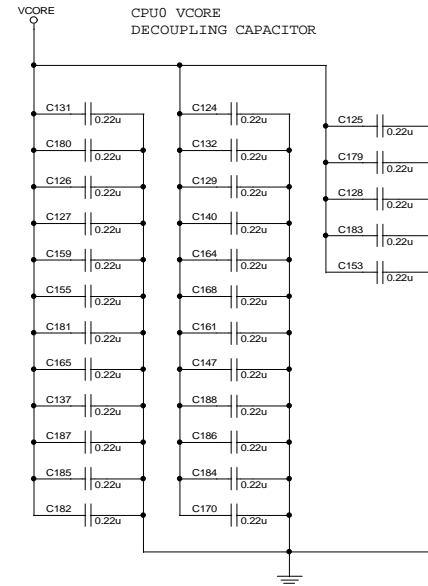
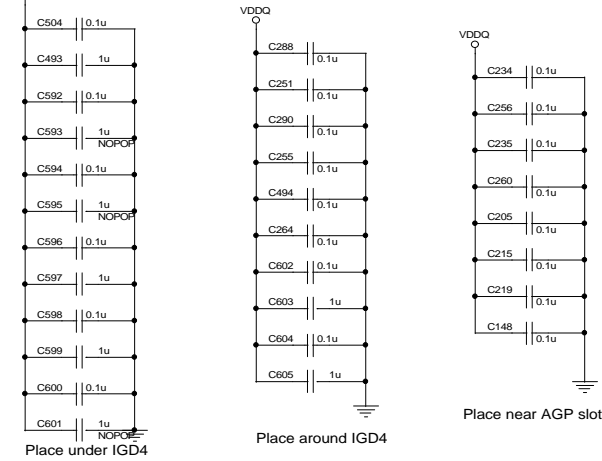


Place at solder side of CPU1

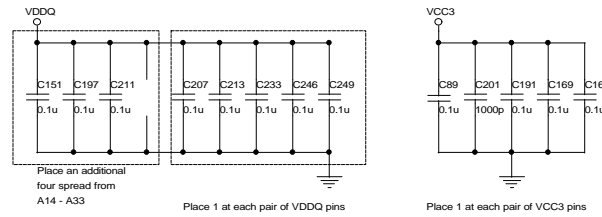


AGP Decoupling

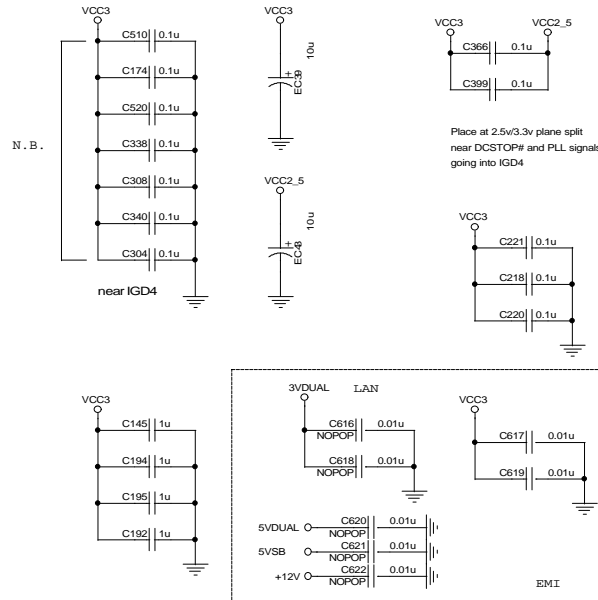
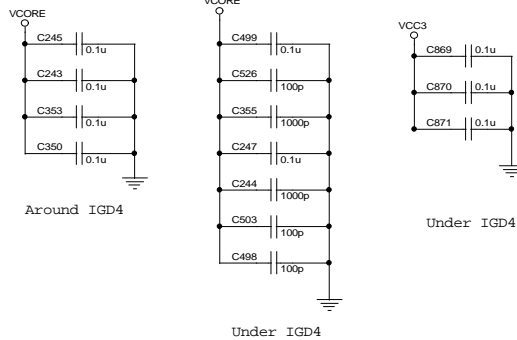
(Near the VDDQ Power Pin of AMD762)



AGP Slot Decoupling

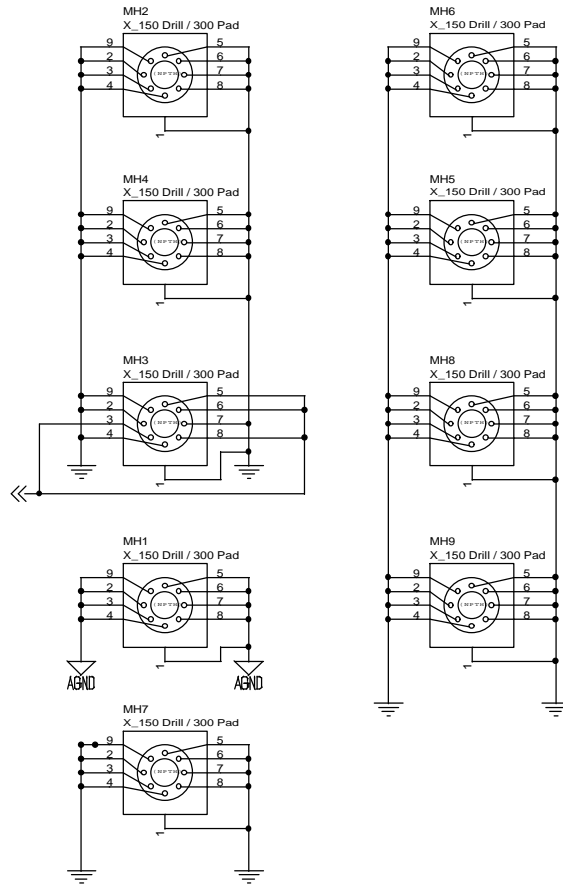


VCCORE decoupling for IGD4

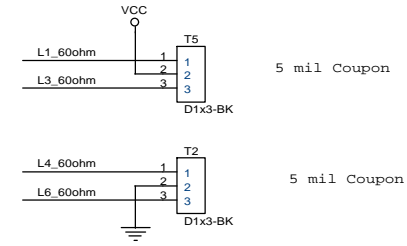
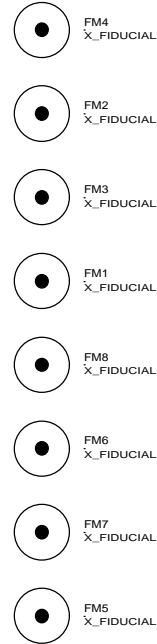


MICRO-STAR			
Bypass Capacitors			
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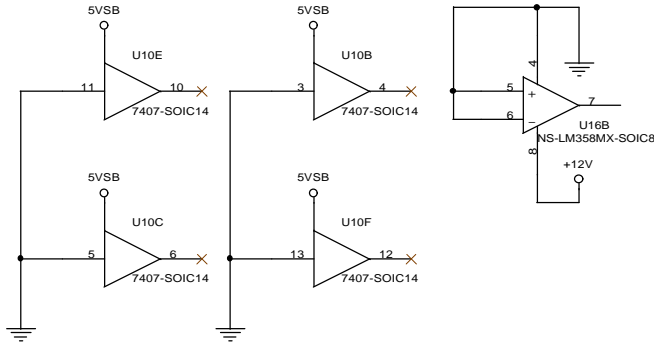
MOUNTING HOLES



FIDUCIALS



24,25,28,32> CGND



MICRO-STAR

Title		
Mounting Hole		
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