

# STAC9750\_MB - Main Board Audio Reference Design Overview

SCOPE: The STAC9750 Main Board reference design provides a complete 2-channel audio solution with digital audio I/O.

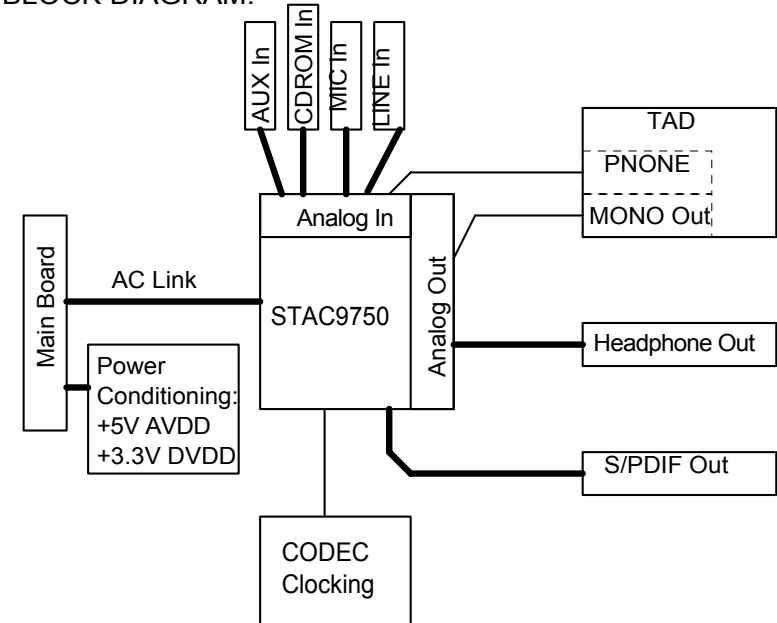
## UNIQUE COMPONENTS:

- 1) STAC9750 Audio Codec with 48-TQFP, 9.0mm tip-to-tip, package.
- 2) 24.576 MHz crystal in Epson MA-306 package, use dual MA-306/CA-301 layout.
- 3) ZR78L05 in SOT-223.
- 4) Radial lead capacitors PCB footprints are listed in PackageDiameter/LeadSpacing/LeadDiameter form.
- 5) EIA prefix footprint surface mount components (EIA abcd) have dimensions of a.b mm by c.d mm.
- 6) SMT prefix footprint surface mount components (SMT wxyz) have dimensions of 0.wx inches by 0.yz inches.


## REVISION HISTORY:

- 1) 7/06/01 - Original release.
- 2) 8/21/01 - Changed PLL mode table for CA3.
- 2) 12/28/01 - changed AFILT caps to 820pF.
- 3) 5/9/03 - Added SPDIF Enable/Disable resistor option.

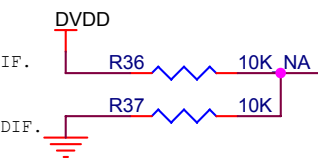
## BLOCK DIAGRAM:



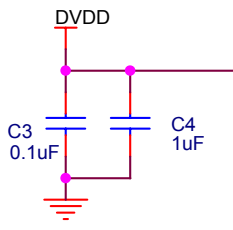
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Title		
<b>Sigmatel Main Board Reference Design Overview</b>		
Size		Rev
A	STAC9750_MB	A3
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INSTALL PULL-UP TO DISABLE SPDIF.  
 INSTALL PULL-DOWN TO ENABLE SPDIF.

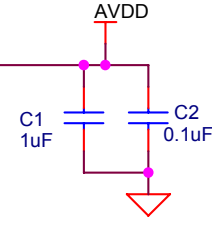


Place 0.1uF decoupling caps as close to Codec as possible.



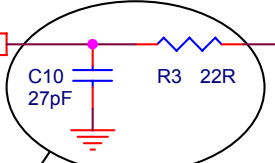
\* Use series resistors on headphone outputs when driving low impedance, highly reactive loads (headphones) to improve amplifier stability.

Place 0.1uF decoupling caps as close to Codec as possible.



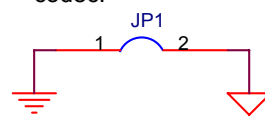
- 7 XTAL\_IN
- 7 XTAL\_OUT
- AC97\_SDATA\_OUT
- AC97\_SDATA\_IN0
- AC97\_SYNC
- 3 CODEC\_RST#
- PCBEEP

AC97\_BITCLK

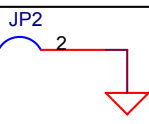


**OPTIONAL EMI FILTER:**  
 Capacitor value selected to minimize high-frequency components in clock output. Capacitor should be selected to critically damp, or slightly under damp the BIT\_CLK signal.

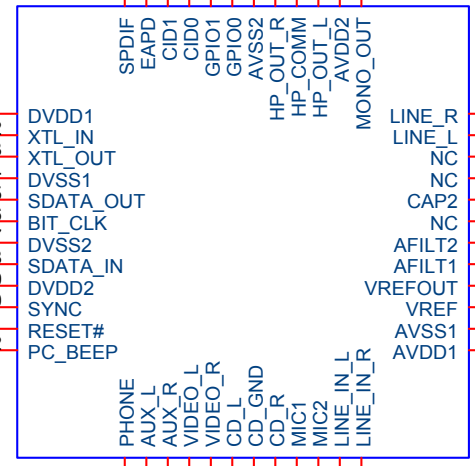
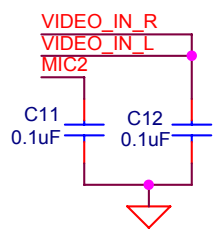
Tie analog and digital grounds together near codec.



Route microphone ground with microphone signal and connect microphone ground to analog ground near codec to reduce noise.

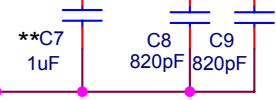


Unused inputs grounded through capacitor.



- SPDIF\_OUT 6
- EAPD 7
- CID1 7
- CID0 7
- GPIO1 6
- GPIO0 6
- HP\_OUT\_R 4
- HP\_OUT\_L 4
- MONO\_OUT 5
- LINE\_OUT\_R 4
- LINE\_OUT\_L 4
- VREFOUT 4
- LINE\_IN\_R 4
- LINE\_IN\_L 4
- MIC2 4
- MIC1 4
- CD\_R 5
- CD\_GND 5
- CD\_L 5
- VIDEO\_IN\_R 5
- VIDEO\_IN\_L 5
- AUX\_IN\_R 5
- AUX\_IN\_L 5
- PHONE 5

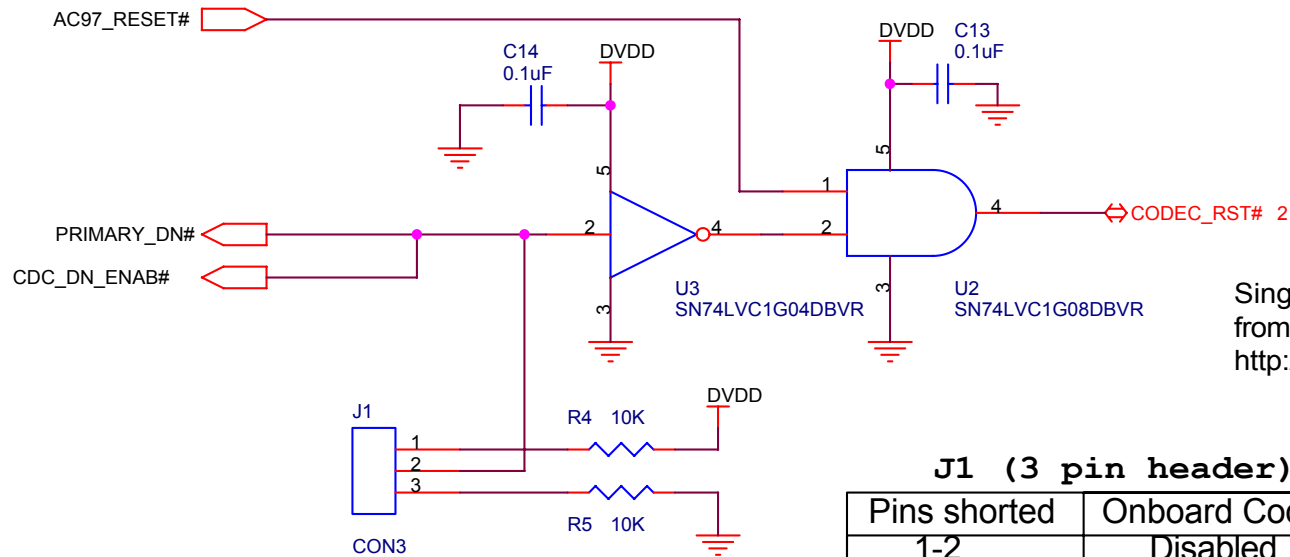
\*\* Vref CAP filters Vref and controls internal anti-pop circuitry. Values greater than 10uF not recommended.



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Title		
<b>STAC9750 AC'97 Audio Codec</b>		
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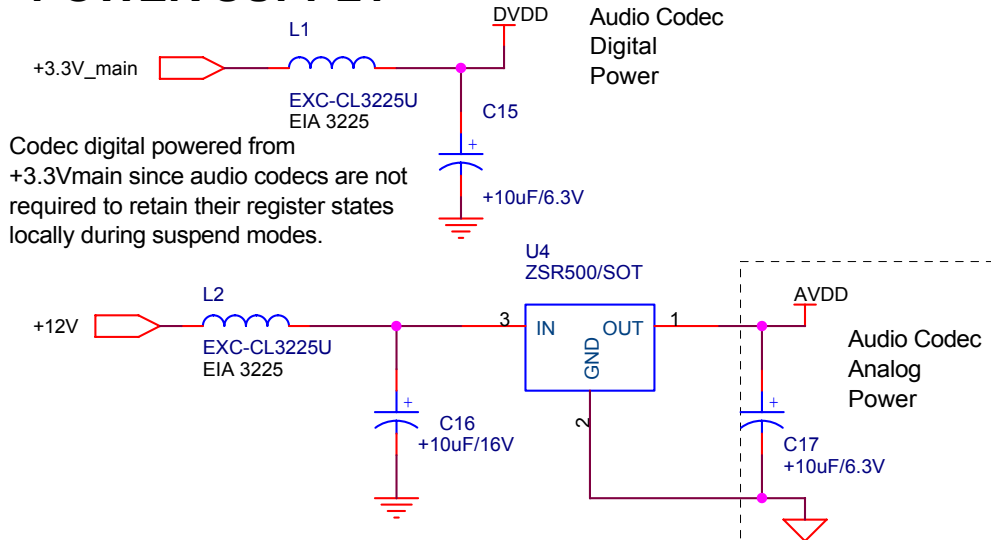
# CODEC DISABLE CIRCUIT



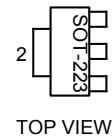
Single Gate devices available from Texas Instruments.  
<http://www.ti.com/>

Pins shorted	Onboard Codec
1-2	Disabled
2-3	Enabled

# POWER SUPPLY



## LAYOUT NOTE FOR ZSR500G:



Device requires large copper pad for proper thermal regulation. Please consult Zetex at <http://www.zetex.com/>

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	Title <b>CODEC DISABLE CIRCUITS</b>	

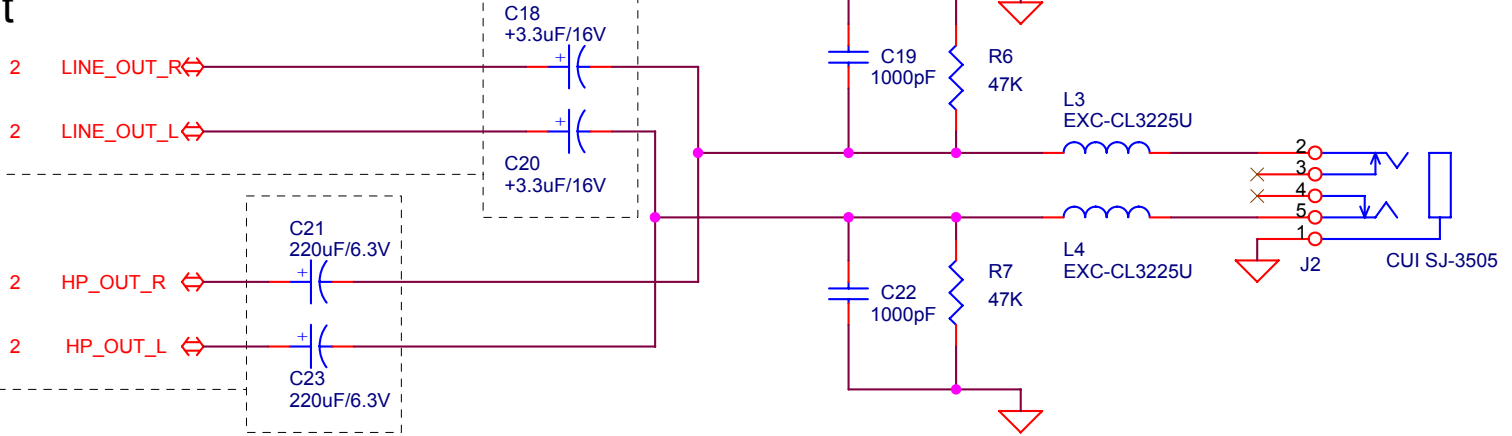
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# Headphone (Line) Out

Primary AC-Coupling Capacitors \*\*\*

Only install one set of capacitors.

Alternate AC-Coupling Capacitors \*\*\*



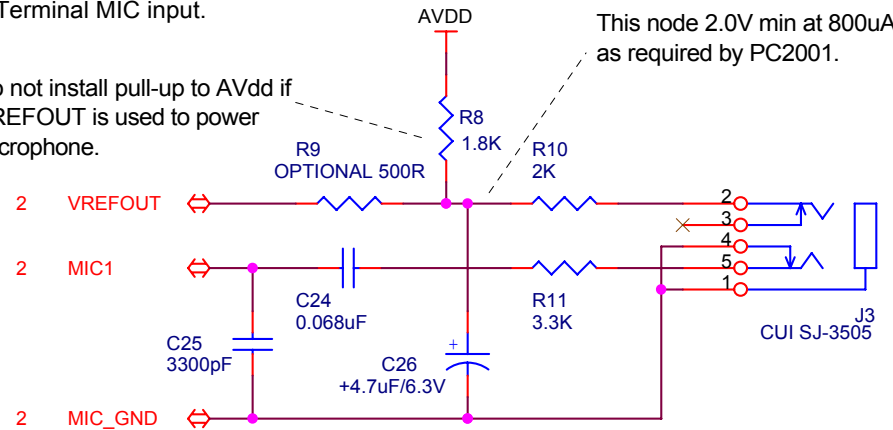
\*\*\* Note: 220uF ac-coupling capacitors will drive loads of 32 ohms and greater and still meet the bandwidth requirements of PC2001. 3.3uF ac-coupling capacitors will drive loads of 10K ohms and greater and still meet the bandwidth requirements of PC2001.

# Microphone Input Circuit

Supports 3-Terminal and 2-Terminal MIC input.

Do not install pull-up to AVDD if VREFOUT is used to power microphone.

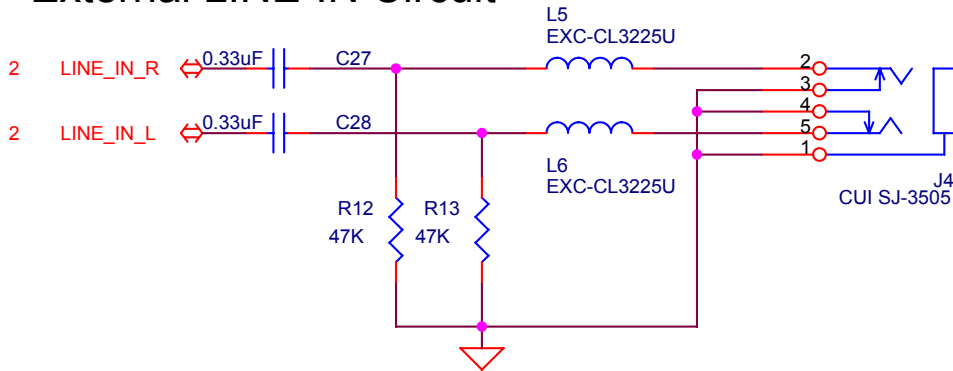
This node 2.0V min at 800uA, as required by PC2001.



Microphone ground should be routed back to codec along with the main microphone signal trace. Improper microphone grounding can result in audible mouse and CDROM noise. Tie MIC\_GND to AGND at a point near the codec.

# REAR PANEL

## External LINE-IN Circuit



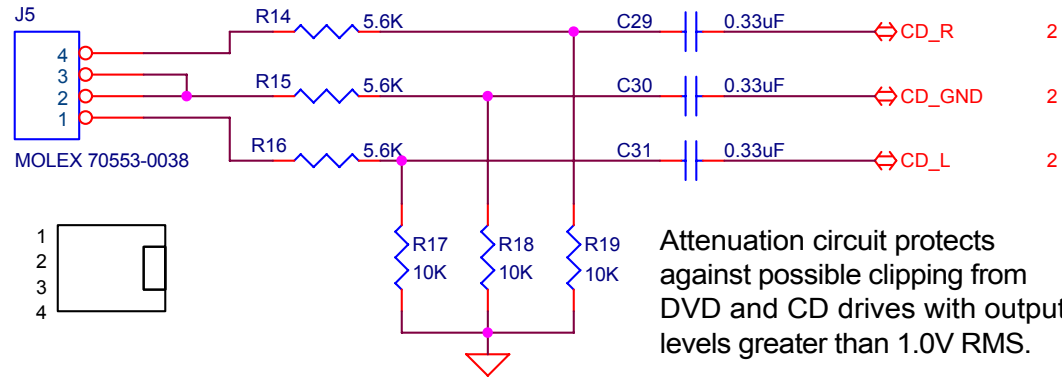
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	Title <h3 style="text-align: center;">Rear Panel Jacks</h3>	

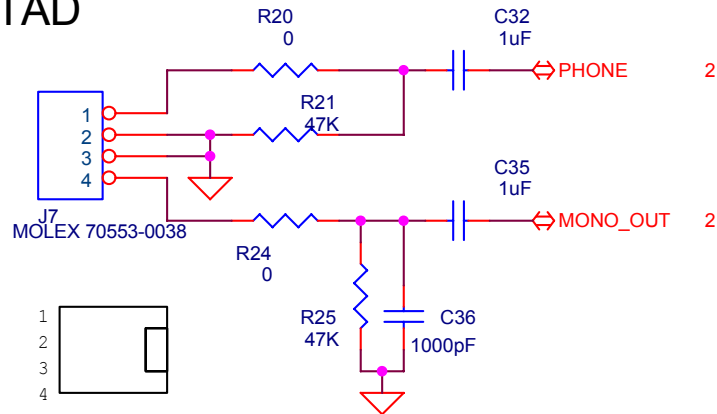
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# INTERNAL AUDIO JACKS

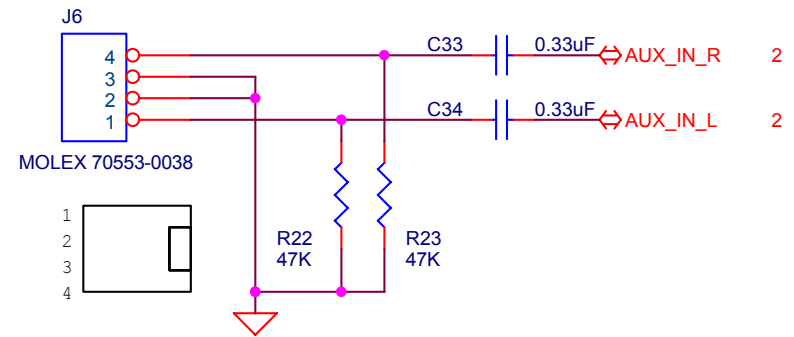
## CDROM Circuit with 4.5dB Attenuation



## TAD



## AUX Input Circuit



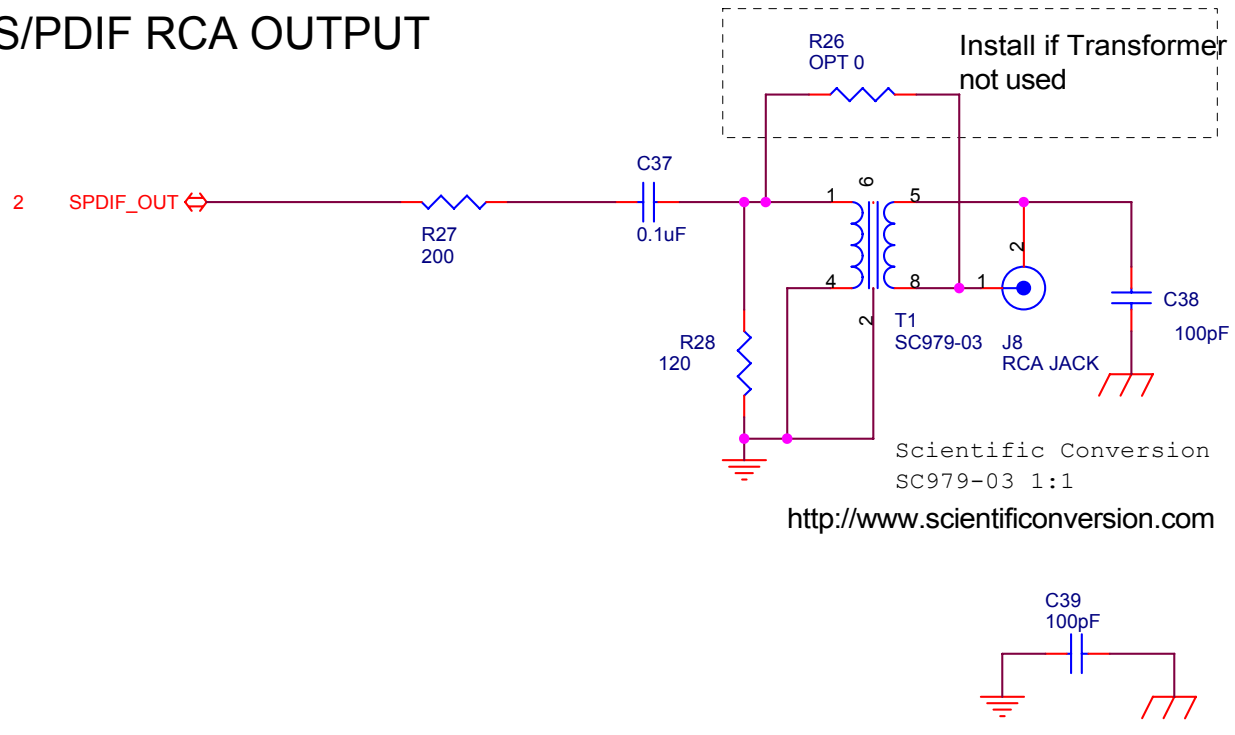
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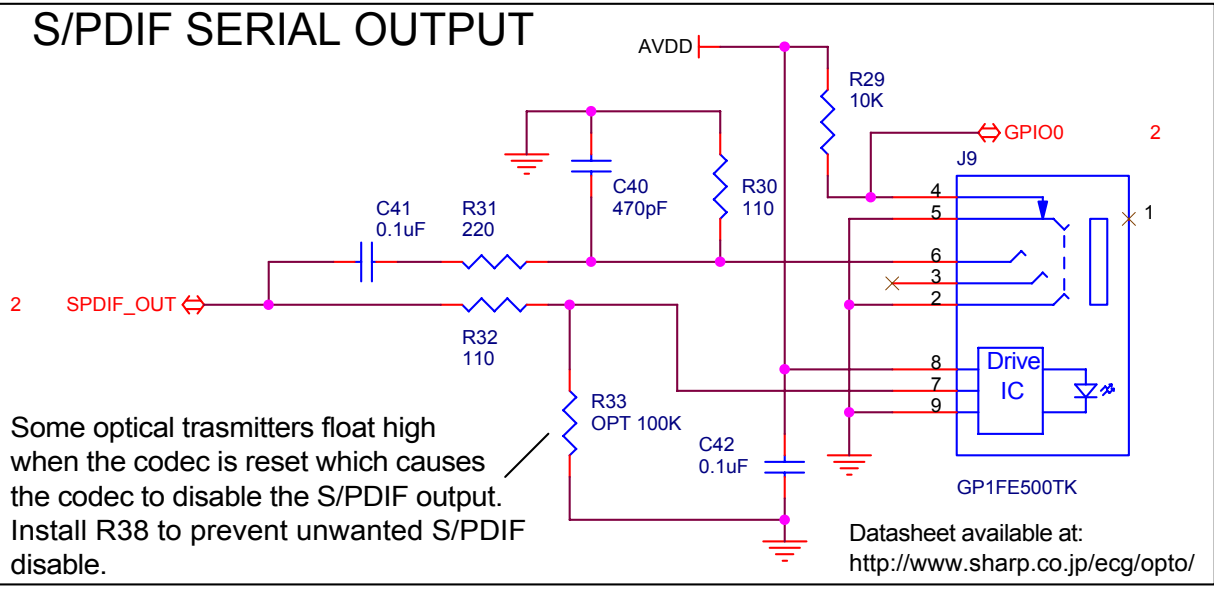
Title		
<b>Analog Audio Jacks</b>		
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# S/PDIF RCA OUTPUT




Please do not populate both the 3.5mm and the RCA SPDIF options.

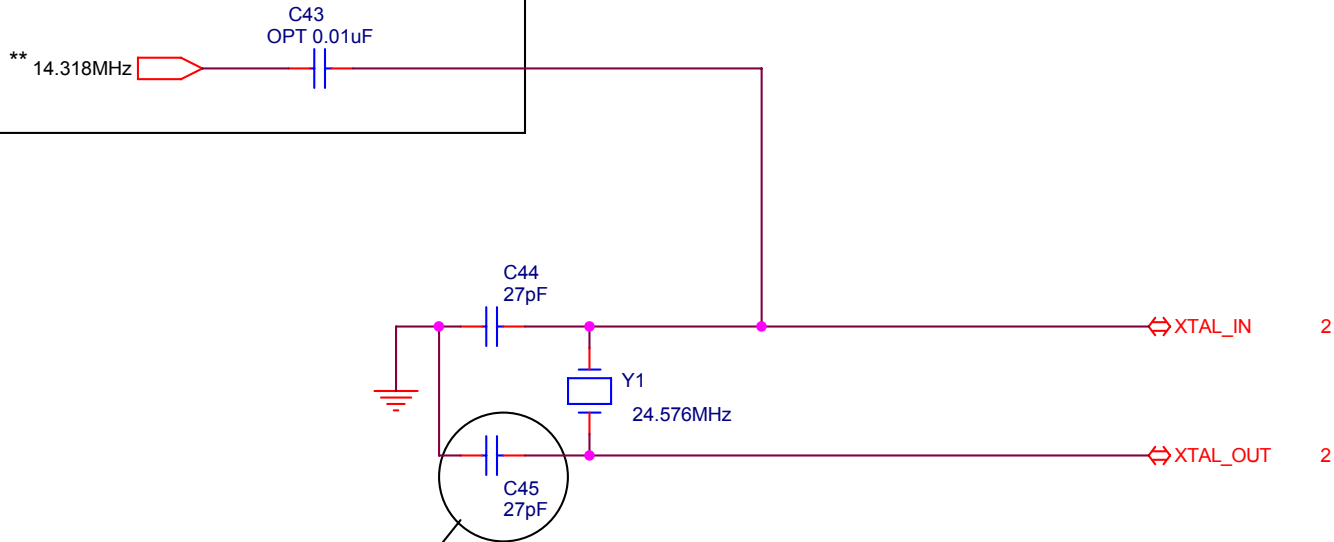
# S/PDIF SERIAL OUTPUT



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Title		
<b>S/PDIF Output</b>		
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Optional Main Board Clock Source  
 Do not populate C44 or Y1 when  
 using an external clock.  
 Replace C45 with 0 ohm resistor  
 SEE TABLE BELOW



Motherboard Clock Frequency determines the CID0/CID1 values when external clock is selected (XTAL\_OUT must be grounded by replacing C45 with a 0 ohm resistor)

Clock Source	R40 CID1	R39 CID0	C45 XTAL_OUT
**14.318 MHz	open	open	GND
27 MHz	open	1K	GND
48 Mhz	1K	open	GND
24.576 MHz	1K	1K	GND



**\*STAC9750 CA1 and CA2 revisions differ from this chart.**



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Title <b>Codec Clocking</b>		
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